Models 585B & 588B Pulsed Microwave Frequency Counters

Operation and Service Manual

EIP Microwave, Inc.
1589 Centre Pointe Drive, Milpitas, CA 95035
TEL: (408) 945-1477
FAX: (408) 945 0977

Manual Assembly Part Number: 5585040-04
Manual Text Part Number: 5580039-03
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585B: CCN 6804
588B: CCN 6905

Warranty

EIP Microwave warrants this product to be free from defects in material and workmanship for three years* from the date of delivery. Damage due to accident, abuse, or improper signal level is not covered by the warranty. Removal, defacement, or alteration of any serial or inspection label, marking, or seal may void the warranty. EIP Microwave will repair or replace, at its option, any components of this product which prove to be defective during the warranty period, provided the entire unit is returned to EIP or an authorized service facility. In-warranty units will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No warranty other than the above is expressed or implied.

Certification

EIP Microwave certifies this instrument to be in conformance with the specifications noted herein at time of shipment from the factory. EIP Microwave further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology.

Instruments Covered by This Manual

The information in this manual applies to EIP Models 25B and 28B with the CCN number(s) listed on the cover. The CCN is the configuration control number. It is a four digit number which is either shown separately as the "CCN" on the serial number tag of the instrument, or as the first four digits of the serial number. The serial number tag is located on the lower rear frame. Please inspect the serial number tag of the instrument and verify the CCN is listed among the CCN numbers covered by this manual.

Manual Updates

The CCN of the instrument will change any time a part or assembly of the instrument is changed to the extent that it is no longer interchangeable with the earlier part or assembly. When changes occur, either a new manual is printed incorporating the changes or the manual is shipped with a Manual Update. To ensure the technical accuracy of the manual, please be sure to incorporate new information as instructed in the Manual Update.

Supplied Accessories

The EIP Models 25B and 28B are supplied with an operations manual, an ac line cord, and a protective front cover. Other available options and accessories are listed in Section 1.

Customer Suggestion Form

A mail-in form at the end of this manual provides an easy way for you to tell us about any additions, corrections, or changes that would improve this publication. Your suggestions are a valuable part of the input used in revising our manuals and developing the structure and format for new manuals.

* Products shipped prior to October 1992 had a standard one year warranty.

SAFETY

The EIP Models 25B and 28B have been designed and tested according to international safety requirements, but as with all electronic equipment, certain precautions must be observed. This manual contains information, cautions, and warnings that must be followed to prevent the possibility of personal injury and/or damage to the instrument.

SAFETY SYMBOLS

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure or practice, which, if not correctly performed or adhered to, could result in personal injury.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

OVERALL SAFETY CONSIDERATIONS

WARNING

Before this instrument is switched on, the protective earth terminals of this instrument MUST be connected to the protective conductor of the ac power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective earth (grounding) conductor.

WARNING

Only fuses with the required rated current, voltage and specified type should be used. DO NOT use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

CAUTION

Before connecting power to the instrument, check to insure that the correct fuse is installed and the voltage select switch on the rear panel of the instrument is set properly. Refer to Section 2, Installation.

CAUTION

Excessive signals can damage these instruments. To prevent damage, do not exceed specified damage level. Refer to specifications listed in Section 1.

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SECTION 1
GENERAL INFORMATION

INTRODUCTION

The EIP Models 585B and 588B Pulsed Microwave Frequency Counters are microprocessor-based multifunction instruments used for both CW and pulsed microwave measurements. They can automatically measure the frequency of repetitive pulse signals as narrow as 50 ns. Both models can also automatically measure pulse widths from 50 ns to 1 second and pulse periods from 250 ns to 1 second, to a 10 ns resolution. Additionally, through the INHIBIT IN connector, the 585B and 588B can profile pulsed or chirped signals with measurement windows as narrow as 15 ns. No manual switching is required to measure CW or pulsed signals.

The frequency range of the 585B is 100 Hz to 20 GHz. The frequency range of the 588B is 100 Hz to 26.5 GHz, and is extendible, by option, up to 170 GHz. Band 0, 100 Hz to 250 MHz, is for CW measurements only.

All major functions are controlled through the 21-button, functionally grouped keyboard. Information is presented for viewing on a nine-digit sectionalized frequency display, a three-digit floating point pulse parameter display, and a 20-message annunciator bank.

Microprocessor control and the unique architecture employed offer all the major counter functions, such as frequency offsets, frequency range limits, and averaging capabilities, plus a variety of special functions including internal diagnostics, calibration and test aids, and sophisticated operational enhancements.

All front panel controls (except the POWER switch) and all background functions are externally programmable via the IEEE 488 - 1978 standard GPIB (General Purpose Interface Bus) port. The instrument output status and all displayed information are accessible via the GPIB.

OPERATING CONDITIONS

This instrument is designed to be operated at temperatures not exceeding 0 to 50 °C at relative humidity not to exceed 95% (75% over 25 °C; 45% over 40 °C). This instrument will perform to specifications at altitudes not exceeding 10,000 ft (3050 m) and will tolerate vibration not exceeding 2 g. It is fungus resistant. The chassis is not designed to provide protection from mechanical shock or falling water particles and is intended for normal bench use in an environmentally uncontaminated area.

VENTILATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce counter stability and shorten component life.

STORAGE

Store the instrument in an environment that is protected from moisture, dust, and other contaminants. Do not expose the instrument to temperatures below -55 °C or above 75 °C, nor to altitudes above 40,000 ft (12,000 m).

SPECIFICATIONS

GENERAL	
SIZE	3.5 in H x 16.75 in. W x 14 in. D (8.9 cm H x 42.6 cm W x 35.6 cm D)
WEIGHT	35 lb (15.9 kg)
SHIPPING WEIGHT	41 lb (18.6 kg)
OPERATING TEMPERATURE	32 to 122 °F (0 to 50 °C)
POWER	100/120/140/200/220/240 Vac ±10% 50-400 Hz, 100 VA, typical
MINIMUM PULSE WIDTH	50 ns
MAXIMUM PULSE WIDTH	CW
MINIMUM PULSE PROFILE	15 ns
MINIMUM PRF	1 Hz
MINIMUM OFF TIME	200 ns (will count CW)
MINIMUM ON/OFF RATIO	15 dB
RESOLUTION	1 kHz to 1 GHz (100 Hz to 100 MHz in Band 0)
GATE TIME	10 ms to 1 µs (dependent upon resolution)

BAND 0	
FREQUENCY RANGE	100 Hz to 250 MHz (CW only)
CONNECTOR	BNC
IMPEDANCE	50 ohms nominal
SENSITIVITY	-15 dBm
MAXIMUM INPUT	+7 dBm
DAMAGE LEVEL	+20 dBm
MAXIMUM VIDEO[1]	N/A
MAXIMUM FM	Carrier frequency must remain within band

(See notes on page 1-7.)

SPECIFICATIONS (Continued)

	BAND 0 (Continued)
AVERAGING ERROR IN Hz	N/A
GATE ERROR IN Hz	N/A
DISTORTION ERROR	N/A
TOTAL ERROR	TE = time base error ±1 count (excluding noise effects)
ACQUISITION TIME	N/A
MEASUREMENT TIME 100 Hz RESOLUTION 1 kHz RES AND ABOVE	 200 ms (1/RES) + 85 ms
	BAND 1
FREQUENCY RANGE	250 MHz to 1 GHz
CONNECTOR	BNC
IMPEDANCE	50 ohms nominal
SENSITIVITY	−15 dBm
MAXIMUM INPUT	+7 dBm peak
DAMAGE LEVEL	+24 dBm peak
AMPLITUDE DISCRIMINATION	10 dB for signals separated by <100 MHz
MAXIMUM VIDEO[1] VIDEO FREQUENCY <250 MHz VIDEO FREQUENCY >250 MHz (SL FREQUENCY MUST BE >250 MHz)	 MV = SL − [10 log (250 MHz/FV)^4] − 20 dB MV = SL − 20 dB
MAXIMUM FM/CHIRP[2]	Carrier frequency must remain within band
AVERAGING ERROR IN Hz[1]	AE = $\pm 2 \times \sqrt{\text{RES}/[(\text{GW})\ (\text{AVG})]}$
GATE ERROR IN Hz[1]	GE = ±0.07/GW
DISTORTION ERROR IN Hz[1]	DE = $\pm 0.03/(\text{PW} - 3 \times 10^{-8})$
TOTAL ERROR (PULSE)[1]	TEp = ±AE ±GE ±DE ±Time Base Error
TOTAL ERROR (CW)	TEcw = Time Base Error ±1 count (Based on averaging 10 measurements.)
ACQUISITION TIME[1]	AQ = (1/MINPRF) + 55 ms
MEASUREMENT TIME (PULSE)[1]	MT = [((4) (PP)) / ((GW) (RES))] +0.1
MEASUREMENT TIME (CW)[1]	MT = [4 / ((GW) (RES))] +0.1

(See notes on page 1-7.)

SPECIFICATIONS (Continued)

	BAND 2
FREQUENCY RANGE	950 MHz to 20 GHz (585B), 26.5 GHz (588B)
CONNECTOR	Precision N (585B), APC 3.5 (588B)
IMPEDANCE	50 ohms nominal
SENSITIVITY	-20 dBm (950 MHz to 20 GHz) -10 dBm (20 to 26.5 GHz, 588B Only)
MAXIMUM INPUT	+7 dBm peak
DAMAGE LEVEL	+45 dBm CW, +53 dBm peak ($\leq$1 μsec pulse width, 0.1% duty cycle)
AMPLITUDE DISCRIMINATION	15 dB. If <15 db, will count one signal accurately if separated by >200 MHz.
MAXIMUM VIDEO[1]	MV = SL - 20 dB
MAXIMUM FM/CHIRP[2]	20 MHz peak-to-peak
AVERAGING ERROR IN Hz[1]	$AE = \sqrt{RES/[(GW)\ (AVG)]}$
GATE ERROR IN Hz[1]	$GE = \pm 0.01/GW$
DISTORTION ERROR IN Hz[1]	$DE = \pm 0.03/(PW - 3 \times 10^{-8})$
TOTAL ERROR (PULSE)	TEp = $\pm$AE $\pm$GE $\pm$DE $\pm$Time Base Error
TOTAL ERROR (CW)	TEcw = Time Base Error $\pm$1 count (Based on averaging 10 measurements)
ACQUISITION TIME (PULSE)	
FREQ. LIMITS	$AQ = 2(FH)[(4 \times 10^{-12}) + (4 \times 10^{-8}/MINPRF)] + 60/MINPRF + [(2 \times 10^{-5})(PP)]/GW + 0.35$
CENTER FREQ	$AQ = 72/MINPRF + [(2 \times 10^{-5})(PP)]/GW + 0.2$
ACQUISITION TIME (CW)	
FREQ. LIMITS	$AQ = 2(FH)[(4 \times 10^{-12}) + (4 \times 10^{-8}/MINPRF)] + 60/MINPRF + 0.25$
CENTER FREQ	$AQ = 72/MINPRF + 0.1$
MEASUREMENT TIME (PULSE)	MT = [(PP) / ((GW) (RES))] + 0.2
MEASUREMENT TIME (CW)	MT = (1/MINPRF) + 0.2
FREQUENCY LIMITS	Instrument will ignore signals outside of limits. 10 MHz resolution, $\pm$50 MHz accuracy. Unwanted signals must be greater than 100 MHz from either limit.
CENTER FREQUENCY	Will lock on signals $\leq$50 MHz from the entered frequency at sensitivity. 10 MHz resolution.

(See notes on page 1-7.)

SPECIFICATIONS (Continued)

	BAND 3 (Option 5804)
FREQUENCY RANGE	26.5 to 170 GHz, see Table 1-1
CONNECTOR	Depends on remote sensor, see Table 1-1
SENSITIVITY	-20 dBm (-25 dBm Typ)
MAXIMUM INPUT (TYP)	+5 dBm peak
DAMAGE LEVEL	+10 dBm peak
AMPLITUDE DISCRIMINATION	20 dB
MAXIMUM VIDEO[1]	MV = 15 mv peak-to-peak
MAXIMUM FM/CHIRP[2] AUTOMATIC CENTER FREQ	 20 MHz peak-to-peak 150 MHz peak-to-peak
AVERAGING ERROR IN Hz[1]	$AE = \pm 2 \times \sqrt{RES/[(GW)(AVG)]}$
GATE ERROR IN Hz[1]	$GE = \pm 0.03/GW$
DISTORTION ERROR IN Hz[1]	$DE = \pm 0.02/(PW - 3 \times 10^{-8})$
TOTAL ERROR (PULSE)	TEp = ±AE ±GE ±DE ±Time Base Error
TOTAL ERROR (CW)	TEcw = Time Base Error $\pm N^2$ counts N = freq/20 GHz
ACQUISITION TIME (PULSE)[1] AUTOMATIC CENTER FREQ	 $AQ = 70/MINPRF + [[(6 \times 10^{-3})(PP)]/GW] + 0.25$ $AQ = 70/MINPRF + [[(8 \times 10^{-4})(PP)]/GW] + 0.25$
ACQUISITION TIME (CW)	AQ = 70/MINPRF + 0.25
MEASUREMENT TIME (PULSE)	MT = [(4)(PP)]/[(GW)(RES)] + 0.15
MEASUREMENT TIME (CW)	(4 / MINPRF) + 0.15
CENTER FREQUENCY	Instrument assumes any signal present to be in the range of ±2 GHz from the specified center frequency and calculates the harmonic number based on this assumption.

(See notes on page 1-7.)

SPECIFICATIONS (Continued)

PULSE PERIOD	
ACCURACY[1]	±(20 ns + time base error x PP)
DISPLAY RESOLUTION	3 digits, floating point, 10 ns maximum (Special function available for 10 ns)
RESOLUTION TO GPIB	10 ns
MIN/MAX PULSE PERIOD	250 ns/1 s
MEASUREMENT POINTS	6 dB ±1.5 dBc
PULSE WIDTH	
ACCURACY[1]	±(20 ns + time base error x PW)
DISPLAY RESOLUTION	3 digits, floating point. 10 ns maximum (Special function available for 10 ns on all measurements)
RESOLUTION TO GPIB	10 ns
MIN/MAX PULSE WIDTH	50 ns/1 s
MEASUREMENT POINTS	6 dB ±1.5 dBc
TCXO TIME BASE (STANDARD)	
FREQUENCY	10 MHz
AGING RATE	$<\|1 \times 10^{-7}\|$ / mo
SHORT TERM STABILITY	$<1 \times 10^{-9}$ RMS for one second averaging time
TEMPERATURE STABILITY	$<\|1 \times 10^{-6}\|$ over the range 0 to 50 °C
LINE VARIATION	$<\|1 \times 10^{-7}\|$ (±10% line voltage change)
WARM-UP TIME	30 minutes
OUTPUT FREQUENCY	10 MHz, square wave, 1 V peak-to-peak minimum into 50 ohms
EXTERNAL TIME BASE	Requires 10 MHz, 1 V peak-to-peak minimum into 300 ohms
PHASE NOISE	-95 dBc/Hz at 10 Hz from carrier

(See notes on page 1-7.)

Note 1: MV is the maximum video amplitude in dBm.
SL is the input signal level in dBm.
FV is the frequency component of the video in Hz.
GW is the logical "AND"of pulse width and inhibit signal minus 30 ns.
PW is pulse width of the incoming signal in seconds.
PP is the period of the input signal in seconds.
RES is the resolution in Hz up to 1 MHz. Above 1 MHz, resolution is 1 MHz.
AVG is the number of measurements averaged.
FH is the difference between Frequency Limit High and Frequency Limit Low in Hz.
MINPRF is the specified instrument MINPRF in Hz up to 1 kHz. Above 1 kHz MINPRF is 1 kHz.

Note 2: If FM/Chirp is >150 MHz and nonsymmetrical, the measured frequency is a function of average frequency and geometric center frequency.

OPTIONS AND ACCESSORIES

OPTIONS	DESCRIPTION
5803	Rear Panel Input Connectors
5804	Band 3 Frequency Extension Module. Available on Model 588B only. Required for frequencies between 26.5 GHz and 170 GHz. Frequency Extension Cable Kit 890 and appropriate remote sensors are also required.
5806	2-Year Extended Warranty①
5807	Ovenized High Stability Timebase (Aging Rate: 5 x 10^{-9}/day)②
5808	Ovenized High Stability Timebase (Aging Rate: 1 x 10^{-9}/day)②
5809	AT-cut Ovenized High Stability Timebase (Aging Rate: 5 x 10^{-10}/day)②
5809	SC-cut Ovenized High Stability Timebase (Aging Rate: 5 x 10^{-10}/day)

ACCESSORIES	DESCRIPTION
890	Frequency Extension Cable Kit
091	Remote Sensor 26.5 - 40 GHz (WR-28)
092	Remote Sensor 40 - 60 GHz (WR-19)
093	Remote Sensor 60 - 90 GHz (WR-120
094	Remote Sensor 90 - 110 GHz (WR-10)
095	Remote Sensor 50 - 75 GHz (WR-150
096	Remote Sensor 33 - 50 GHz (WR-22)
097	Remote Sensor 26.5 - 50 GHz (Coaxial K-Connector③)
098	Remote Sensor 110 - 170 GHz (WR-6)
010	Transit Case
021	Rack Mount Kit with Handles
022	Rack Mount Kit without Handles
031	Operation Manual (one supplied with each instrument)
032	Service Manual (includes Operation Manual)
041	Service Kit
050	Sof-Pac Carrying Case
101	Chassis Slide Kit with Handles (includes rack mount kit)
102	Chassis Slide Kit without Handles (includes rack mount kit)

① A three year warranty became standard as of October 1, 1992.

② Options 5807, 5808, and 5809 were discontinued as of December 1992. These discontinued high stability ovenized oscillators incorporated an AT-cut crystal. They were replaced by a new Option 5809 incorporating a SC-cut crystal. The new Option 5809 has virtually identical specifications as the old Option 5809, but requires less warm-up time.

③ K-Connector is a registered trademark of the Wiltron Company.

Table 1-1. Band 3 Remote Sensors.

REMOTE SENSOR	BAND	FREQUENCY RANGE (GHz)	WAVEGUIDE SIZE	WAVEGUIDE FLANGE	POWER RANGE (dBm)	DAMAGE LEVEL (dBm)
91	3-1	26.5 - 40	WR-28	UG-599/U	-20 to +5	+10
92	3-3	40 - 60	WR-19	UG-383/U	-20 to +5	+10
93	3-5	60 - 90	WR-12	UG-387/U	-15 to +5	+10
94	3-6	90 - 110	WR-10	UG-387/U	-15 to +5	+10
95	3-4	50 - 75	WR-15	UG-385/U	-20/-15 to +5	+10
96	3-2	33 - 50	WR-22	UG-383/U	-20 to 5	+10
97	3-1 or 3-2	26.5 - 50	K-Connector*	N/A	-20 to +5	+10
98	3-8	110 - 170	WR-6	UG-387/U	-15 to +5	+10

* K-Connector is a registered trademark of the Wiltron Corporation.

Table 1-2. Options 5807, 5808, and 5809 - Ovenized High Stability Timebases (AT-Cut).

	5807	5808	5809
AGING RATE/24 HOURS (After 72 hour warm-up)	$<5 \times 10^{-9}$	$<1 \times 10^{-9}$	$<5 \times 10^{-10}$
SHORT TERM STABILITY (1 second average)	$<1 \times 10^{-10}$ rms	$<1 \times 10^{-10}$ rms	$<1 \times 10^{-10}$ rms
0 to +50 °C TEMPERATURE STABILITY	$<6 \times 10^{-8}$	$<3 \times 10^{-8}$	$<3 \times 10^{-8}$
±10% LINE VOLTAGE CHANGE	$<5 \times 10^{-10}$	$<2 \times 10^{-10}$	$<2 \times 10^{-10}$

Table 1-3. Option 5809 - Ovenized High Stability Timebase (SC-Cut).

FREQUENCY	10 MHz
AGING RATE	$<5 \times 10^{-10}$/24 hours (after one hour warm-up), 1×10^{-7}/year
SHORT TERM STABILITY (1 second average)	$<1 \times 10^{-10}$ rms
0 to +50 °C TEMPERATURE STABILITY	$<3 \times 10^{-8}$
±10% LINE VOLTAGE CHANGE	$<2 \times 10^{-10}$
WARM-UP TIME	Within $\leq 5 \times 10^{-9}$ of final value 10 minutes after turn-on at 25 °C Within 1×10^{-9} of final value 30 minutes after turn-on at 25 °C
PHASE NOISE	-120 dBc/Hz at 10 Hz from carrier

Note: Options 5807, 5808, and 5809 were discontinued as of December 1992. These discontinued high stability ovenized oscillators incorporated an AT-cut crystal. They were replaced by a new Option 5809 incorporating a SC-cut crystal. The new Option 5809 has virtually identical specifications as the old Option 5809, but requires less warm-up time.

The older Options 5807, 5808, and 5809 (AT-cut) are adjusted using a rear panel adjustment. The adjustment for the new Option 5809 (SC-cut) is inside the counter beneath a screw on top of the oscillator.

SECTION 2
INSTALLATION

UNPACKING

The EIP Models 585B and 588B series Pulsed Microwave Frequency Counters arrive ready for operation. Carefully inspect the shipping carton for any sign of damage. If the carton is damaged, immediately notify shipper's agent.

Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the counter, checking for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

INSTALLATION

There are no special installation instructions for these units. The units are self-contained bench or rack mounted instruments, which only require connection to a standard, single-phase power line for operation.

CAUTION

Always be sure that the fuse is the type and value specified, and that the voltage select switch (Figure 2-1) is set to correspond to the AC power input voltage; otherwise, the counter may be damaged.

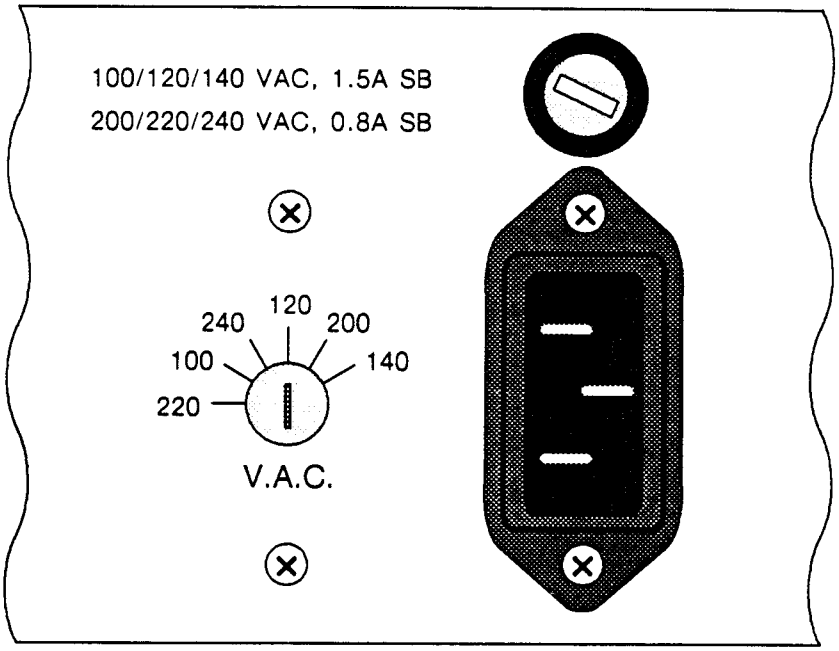

Figure 2-1. Rear Panel Fuse and Voltage Select Switch Locations.

VOLTAGE SELECTION

The voltage select switch (V.A.C.) must be set to the proper line voltage. To change the line voltage, disconnect the counter from the power line and, using a screwdriver, set the V.A.C. switch to the desired position.

FUSE REPLACEMENT

The fuse for the counter is located on the rear panel above the line voltage socket (Figure 2-1). The following fuse types must be used:

Line Voltage	Fuse Type
100/120/140 Vac	1.5 A Slow-blow MDL
200/220/240 Vac	0.8 A Slow-blow FST

To release the fuse, use a screwdriver to rotate the slotted cap counterclockwise. To reinstall the fuse, press the fuse and slotted cap assembly into the fuse cavity and turn it clockwise until it locks into place.

INCOMING OPERATIONAL CHECKOUT

The following procedure can be performed without special tools or equipment.

1. Before connecting power to the instrument, check to make sure the correct fuse is installed and the V.A.C. switch is set properly.

2. Connect the power cord to the appropriate single-phase power source. The ground terminal on the power cord plug must be properly grounded.

3. Turn the POWER switch on. All LEDs and annunciators should light for about two seconds. The model number should be displayed for about one second. The counter should then display all zeros indicating that the automatic self-check has been successfully completed.

4. Press: SPECIAL 9 FUNC, 0, 1 — Display should read 100 000 ±1 (100 MHz)

5. Press: SPECIAL 9 FUNC, 0, 2 — Display should read all 8's and all annunciators should be lit.

6. Press: SPECIAL 9 FUNC, 0, 3 — Each display segment should light in turn (adjustable by the front panel SAMPLE RATE control).

7. Press: SPECIAL 9 FUNC, 0, 4 — Each digit should light in turn (adjustable by the front panel SAMPLE RATE control).

This completes the incoming operational checkout procedure.

SERVICE INFORMATION

PERIODIC MAINTENANCE

No periodic maintenance is required. However, to maintain accuracy, it is recommended that the counter be recalibrated every 12 months. The specific calibration interval depends upon the measurement accuracy required. For sample measurement error calculations for both 6- and 12-month calibration intervals, see page 3-18.

CAUTION

Do not attempt repair or disassembly of the microwave converter, millimeter wave converter, or time base oscillator assemblies. Such action will void the warranty of the counter. Contact EIP or your sales representative.

COUNTER IDENTIFICATION

This counter is identified by three sets of numbers: the model number (585B or 588B), serial number, and a configuration control number (CCN). These numbers, located on a label affixed to the frame at the rear of the counter, must be included in any correspondence regarding your counter.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model, complete serial number, and CCN of the counter.
- A complete description of the problem. (Under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptoms?)
- Name and telephone number of someone familiar with the problem that may be contacted by EIP for any further information if necessary.
- Shipping address to which the counter is to be returned. Include any special shipping instructions.

Pack the counter for shipping as detailed below.

SHIPPING INSTRUCTIONS

Wrap the counter in heavy plastic or kraft paper, and repack in original container if available. If the original container cannot be used, use a heavy (275 pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the cover of this manual.

SECTION 3
OPERATION

INTRODUCTION

This section lists the counter controls, connectors, and indicators, explains how each counter function operates, and provides some general measurement considerations.

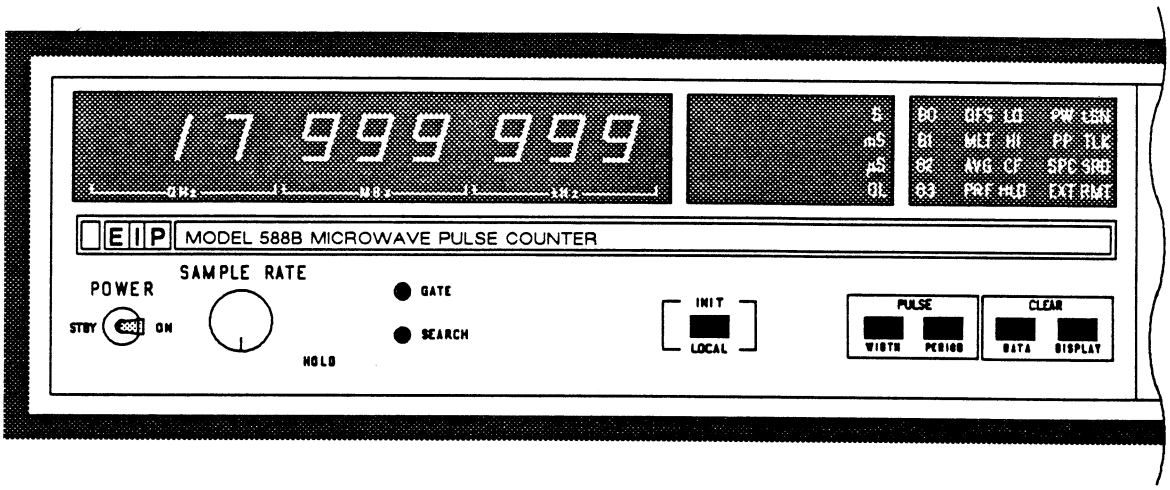

Figure 3-1. Front Panel Controls and Indicators (Model 588B Shown).

FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

- POWER switch - selects ON or STBY. In the standby position power is applied to the oven oscillator, if installed, and to the primary side of the power transformer.
- SAMPLE RATE/HOLD control - varies time between measurements from 0.1 to 10 seconds (nominal). The last reading is retained indefinitely in HOLD.
- GATE indicator - lights when the signal gate is open and a measurement is being made.
- SEARCH indicator - lights when the counter is not locked to an input signal.
- Data display - 12-digit LED display provides a direct numerical readout of a measurement. The frequency information is displayed on the nine left-most digits in a fixed position format that is sectionalized in GHz, MHz, kHz. Pulse parameters (pulse width and pulse period) are displayed in a three-digit floating point format to the right of the frequency display.
- Status display - A series of annunciators provided to indicate current operating status of the counter.
- Keyboard - Both data entry and function selection are controlled through the keyboard (see Keyboard Operation on page 3-5).

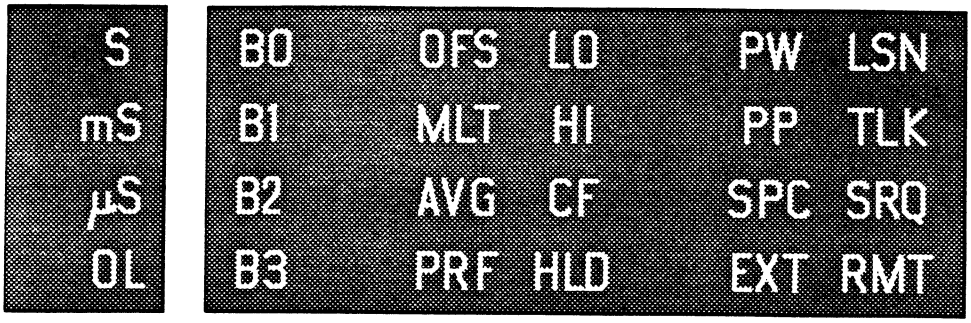

Figure 3-2. Status Display.

STATUS DISPLAY

- S – indicates pulse parameters are being displayed in seconds.
- mS – indicates pulse parameters are being displayed in milliseconds.
- µS – indicates pulse parameters are being displayed in microseconds.
- OL (overload) – indicates that the input signal level is in excess of the optimum counting range. (Overload does not indicate improper operation, only that the input amplitude is greater than optimum.)
- B0 – lights when Band 0 is selected.
- B1 – lights when Band 1 is selected.
- B2 – lights when Band 2 is selected.
- B3 – lights when Band 3 is selected.
- OFS (frequency offset) – lights when a frequency offset is being used.
- MLT (frequency multiplier) – lights when a frequency multiplier other than 1 is being used.
- AVG (average) – lights when measurement averaging is enabled.
- PRF (minimum pulse repetition frequency) – lights when a MINPRF other than the factory default is being used.
- LO (frequency limit low) – lights when a low limit other than the factory default is being used.
- HI (frequency limit high) – lights when a high limit other than the factory default is being used.
- CF (center frequency) – lights when the center frequency mode of operation is enabled.
- HLD (hold) – lights when measurement updating is disabled.
- PW (pulse width) – lights when the counter is in the pulse width measurement mode.
- PP (pulse period) – lights when the counter is in the pulse period measurement mode.
- SPC (special function) – lights when a special function is enabled.
- EXT (external reference) – lights when the counter is set to an external time base reference.

NOTE

For proper counter operation: when the EXT function is selected, a 10 MHz external reference MUST be applied to the rear panel input connector.

GPIB Status Indicators

- LSN (listen) – lights when the counter is addressed as a listener by the GPIB.
- TLK (talk) – lights when the counter is addressed as a talker by the GPIB.
- SRQ (service request) – lights when the counter is sending a service request.
- RMT (remote) – lights to indicate that the front panel controls are disabled and the counter is being controlled by the GPIB.

SIGNAL INPUT CONNECTORS

- BAND 0 (BNC female) – has a nominal input impedance of 50 ohms and is used for CW measurements in the range of 100 Hz to 250 MHz.
- BAND 1 (BNC female) – has a nominal input impedance of 50 ohms and is used for measurements in the range of 250 MHz to 1 GHz.
- BAND 2 (precision N for Model 585B, APC 3.5 female for Model 588B) – has a nominal input impedance of 50 ohms and is used for measurements in the range of 950 MHz to 20 GHz (26.5 GHz for 588B).
- BAND 3 (Optional – for Model 588B only, Selectro "quick connect") – has a nominal input impedance of 50 ohms and is used for measurements in the range of 26.5 to 170 GHz. This input is used in conjunction with the Model 890 Frequency Extension Cable Kit and a remote sensor.

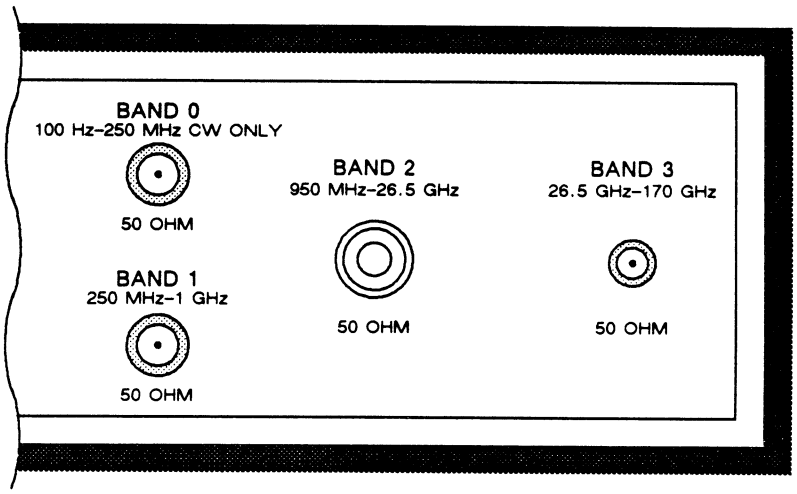

Figure 3-3. Signal Input Connectors (Model 588B Shown).

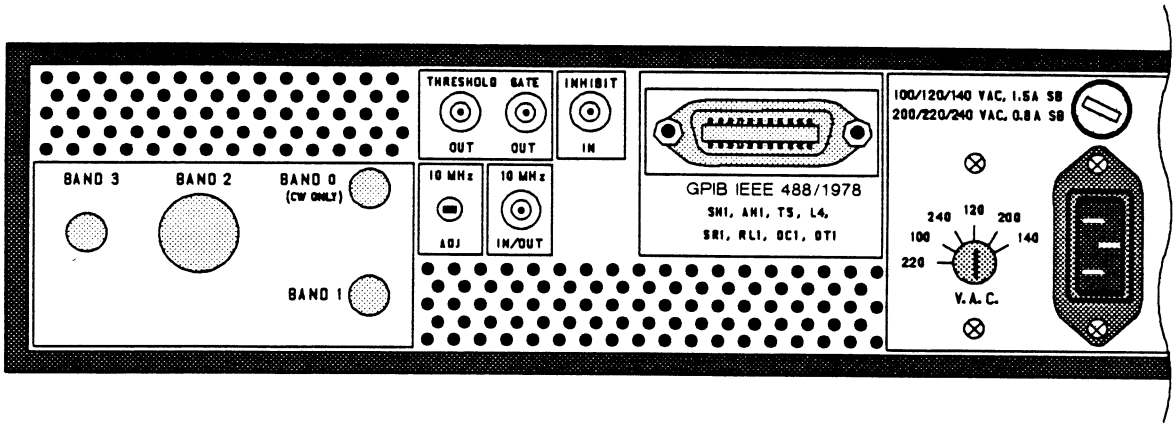

Figure 3-4. Rear Panel Control and Connectors.

REAR PANEL CONTROL AND CONNECTORS

- BAND 0, BAND 1, BAND 2, and BAND 3 - are provided on instruments with optional rear panel inputs (Option 5803).

- THRESHOLD OUT - is the digitized pulse envelope. When the counter has a converter lock and a signal is present, the output is -0.75 volts into 50 ohms. Without a converter lock, the output is 0 volts.

- GATE OUT - represents the gate to the Count Chain board. The gate output follows the actual gate, not the gate enable. When the gate is active, the output is-0.75 volts into 50 ohms; otherwise, the output is 0 volts.

- 10 MHz IN/OUT - provides a 10 MHz square wave output at 1 volt peak-to-peak, AC coupled into 50 ohms, when the counter's internal time base is enabled. Accepts a 10 MHz 1 volt peak-to-peak signal into 300 ohms for external time base operation. Special Functions 08 and 09 are used to select either the external or internal time base.

- INHIBIT IN - causes the counter to perform as if the input signal were turned off. The counter ignores any signal that is present while inhibit is true during all phases of operation. An input of -1 volt inhibits the counter. An input of -2 volts enables the counter. The inhibit input impedance is 50 ohms to -2 volts so that the counter can be driven by either an ECL signal or a 0 to -1 volt, 50 ohm source.

NOTE

The INHIBIT IN is designed to be compatible with either a 50 ohm impedance pulse generator, or emitter-coupled-logic (ECL) devices. An internal termination of 50 ohms returned to -2 volts makes this dual compatibility possible. An ECL high level signal (-0.8 to -1.1 volts) will inhibit measurement. ECL devices are designed to drive 50 ohm lines without reflections when the lines are terminated with 50 ohm returned to -2 volts. The direct compatibility with a 50 ohm pulse generator results from the fact that 0 volts from a 50 ohm source will produce -1 volts at the INHIBIT IN (inhibiting the counter) while a -1 volt signal into 50 ohms will produce 1.5 volts at the INHIBIT IN, thus enabling the counter.

- GPIB - connects the instrument to the IEEE 488 - 1978 bus.
- Fuse - provides current overload protection.
- V.A.C. switch - sets operating voltage of counter to match power line voltage.

CAUTION

Switch setting and fuse rating must match power line voltage.

- AC power connector - accepts the power cord supplied with the counter.

INSTRUMENT DEFAULT SETTINGS

When the counter is initially turned on the state of the counter is determined by a set of default values which are stored in memory. The factory-set values are listed below.

Parameter	Default Value
Band	2 (microwave band)
Subband	1
Resolution	3 (1 kHz)
Special Function	00 (all cleared)
Average	01
Frequency Multiplier	01
Frequency Offset	0 kHz
Minimum PRF	2 kHz
Frequency Limit Low	900 MHz
Frequency Limit High	20.5 GHz (Model 585B) 26.7 GHz (Model 588B)
Center Frequency	0 kHz (not active)
Frequency Display	On
Pulse Width Measurements	Off
Pulse Period Measurements	Off

Models 585B and 588B both offer a feature that enables the user to customize the state of the instrument at turn-on. For more information on this feature, see Special Function 72.

KEYBOARD OPERATION

The keyboard consists of 21 push-button keys that control the major functions of the counter. Twelve keys are used for numerical data entry — the digits 0 through 9, the decimal point, and the change sign (±). Four keys (GHz, MHz, kHz, and Hz) act as terminators for the input of frequency parameters. The CLEAR DISPLAY and CLEAR DATA keys are also considered terminator keys.

Ten of the keys, called parameter call keys, are also used to select the measurement parameters. Five of these, BAND (which also calls subband), SPECIAL FUNC, FREQ MULT, RES, and AVG, are used without terminators, while the other five, MIN PRF, FREQ LIMIT LOW, FREQ LIMIT HIGH, CENTER FREQ, and FREQ OFFSET, are used with the terminator keys. The parameter call keys are dual function keys since they are also used for numeric data entry.

The remaining keys are called one-shot action keys; they include INIT/LOCAL, PULSE PERIOD, PULSE WIDTH, RESET, and TRIG.

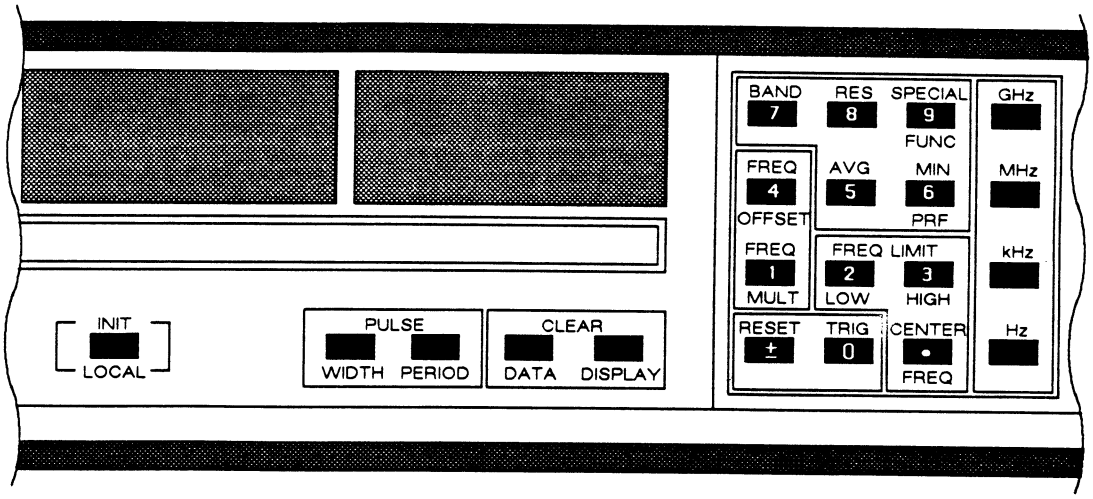

Figure 3-5. Keyboard.

NUMERIC ENTRY KEYS

The numeric entry keys are:

- Digits 0 through 9
- (±) change sign key
- (.) decimal point key

TERMINATOR KEYS

The terminator keys are:

- GHz
- MHz
- kHz
- Hz

Clear Display and Clear Data

These are also considered terminator keys. At any point during a key sequence, the user has the option either to:

- Press CLEAR DISPLAY to abort the sequence and return to normal operation without changing the value of the called parameter.
- Press CLEAR DATA to abort the sequence and assign the default value to the called parameter.

ONE-SHOT ACTION KEYS

- INIT/LOCAL – when the counter is in local mode, this key causes the counter to be initialized to the power-on state. When the counter is in remote mode, the INIT/LOCAL key causes a return to local mode (unless a GPIB local lockout is active).

- PULSE WIDTH – turns the pulse width measurement on or off. The result is displayed in the pulse parameter display.
- PULSE PERIOD – turns the pulse period measurement on or off. The result is displayed in the pulse parameter display.

NOTE

When the counter is in local mode, it cannot display both pulse width and pulse period simultaneously; in remote operation, however, both parameters can be output to the controller.

- RESET – resets the converter and restarts the signal acquisition process. If a signal is found, a measurement will be taken, even if the counter is in HOLD.
- TRIG – begins a new measurement cycle. If a measurement cycle is in progress, it will be aborted.

PARAMETER CALL KEYS

The operation of the counter is controlled by the values of the measurement parameters. These parameters can be changed by the user through the keyboard or via the GPIB.

Parameter Call Keys Used Without Terminator

BAND

This key controls the frequency measurement range. Select the appropriate band according to the following:

Band	Range
0	100 Hz to 250 MHz
1	250 MHz to 1 GHz
2	950 MHz to 20 GHz (Model 585B) 950 MHz to 26.5 GHz (Model 588B)
3	26.5 to 170 GHz (Optional – Model 588B only)

Keyboard Example:

PRESS: BAND, CLEAR DATA to select default band.

PRESS: BAND, 2 to select Band 2.

GPIB Example:

Enter: OUTPUT 718;"BAND 2" to select Band 2.

Subband (Called using BAND key)

This parameter controls the frequency measurement range of Band 3. It is set according to the remote sensor being used. Select the appropriate subband as follows:

Subband	Range (GHz)
1	26.5 to 40
2	33 to 50
3	40 to 60
4	50 to 75
5	60 to 90
6	75 to 110
7	90 to 140
8	110 to 170

Keyboard Examples:

PRESS: BAND [3] CLEAR/DATA to select default subband.

PRESS: BAND [3] [4] to select Band 3, subband 4.

PRESS: BAND CLEAR/DISPLAY to display the band without changing it.

PRESS: BAND [3] CLEAR/DISPLAY to display the subband without changing it.

GPIB Examples:

Enter: OUTPUT 718;"BAND 3, SUBBAND 4" to select Band 3, subband 4.

Enter: OUTPUT 718;"SUBBAND 4" to select subband 4 (if counter is already in Band 3.)This command does not automatically set counter to Band 3.

RES

This key controls the frequency measurement resolution. Select the desired resolution according to the table below.

Resolution	Frequency	Gate Time
2	100 Hz	10 ms (Band 0 only)
3	1 kHz	1 ms
4	10 kHz	100 µs
5	100 kHz	10 µs
6	1 MHz	1 µs
7	10 MHz	1 µs
8	100 MHz	1 µs
9	1 GHz	1 µs

Keyboard Examples:

PRESS: RES, CLEAR DATA to select default resolution.

PRESS: RES, 2 to select resolution 2 (100 Hz).

PRESS: RES, 9 to select resolution 9 (1 GHz).

GPIB Example:

Enter: OUTPUT 718;"RESOLUTION 2" to select resolution 2 (100 Hz).

SPECIAL FUNC

This key is used to call any of the various special functions listed in the Special Functions section of this manual.

Keyboard Examples:

PRESS: SPECIAL FUNC, CLEAR DATA to clear all activated special functions.

PRESS: SPECIAL FUNC, 0, 1 to activate Special Function 01, 100 MHz self-test.

PRESS: SPECIAL FUNC, 0, 4 to activate Special Function 04, scan digits test.

GPIB Example:

Enter: OUTPUT 718; "SPECIAL 01" to activate Special Function 01,100 MHz self-test.

AVG

This key controls the number of measurements to be averaged on frequency and pulse parameters. Select average in the range of 01 to 99.

Keyboard Examples:

PRESS: AVG, CLEAR DATA to select default average factor.

PRESS: AVG, 0, 2 to average 2 readings before displaying the result.

PRESS: AVG, 2, 7 to average 27 readings before displaying the result.

GPIB Example:

Enter: OUTPUT 718;"AVERAGE 27" to average 27 readings before displaying the result.

FREQ MULT

This key controls the value of the constant M in the formula:

Display frequency = (M x measured frequency) ±B

where M is the frequency multiplier and B is the frequency offset. The frequency multiplier must be an integer in the range of 01 to 99.

Keyboard Examples:

PRESS: FREQ/MULT CLEAR/DATA to select the default multiplier value.

PRESS: FREQ/MULT 0 7 to select a multiplier value of 7.

PRESS: FREQ/MULT 3 1 to select a multiplier value of 31.

GPIB Example:

Enter: OUTPUT 718;"MULTIPLIER 31" to select a multiplier value of 31.

Parameter Call Keys Used With Terminator

FREQ OFFSET

Frequency offset allows the entry of a negative or positive frequency to 1 kHz resolution into the offset frequency register. This parameter controls the constant B in the formula:

Displayed frequency = (M x measured frequency) ±B

where M is the frequency multiplier and B is the frequency offset. Select frequency offset in the range of -99.999 999 GHz to +99.999 999 GHz. The number can be entered in any fixed-point format. The units terminator determines the scale of the input number.

Keyboard Examples:

PRESS: FREQ/OFFSET CLEAR/DATA to select the default value.

PRESS: FREQ/OFFSET 1 2 . 3 4 MHz to select a 12.34 MHz value.

PRESS: FREQ/OFFSET ± 0 . 1 2 GHz to select a -0.12 GHz value.

GPIB Example:

Enter: OUTPUT 718;"OFFSET 12.34 MHZ" to select a 12.34 MHz value.

MIN PRF

This key controls the minimum pulse repetition frequency of the pulsed signals that can be acquired and measured by the counter. For example, if a MIN PRF of 500 Hz is selected, the

counter will only measure signals with a minimum pulse repetition frequency of 500 Hz or greater. This parameter affects the acquisition speed indirectly by affecting two internal processes: the time of waiting for a pulse at each frequency step in the frequency range search, and the time of waiting for a pulse when taking measurements before declaring a "signal lost" condition.

Select MIN PRF in the range of 1 Hz to 100 kHz, depending on the minimum pulse repetition frequency of the signal being measured. The number can be entered in any fixed-point format; the units terminator determines the scale of the input number.

Keyboard Examples:

PRESS: MIN PRF, CLEAR DATA to select the default value.

PRESS: MIN PRF, 5, 0, 0, Hz to select a 500 Hz value.

GPIB Example:

Enter: OUTPUT 718;"MINPRF 500 HZ" to select a minimum pulse repetition frequency value of 500 Hz.

FREQ LIMIT LOW

This key controls the low end of the frequency window that is searched for a signal in Band 2. Select frequency limit low in the range of 900 MHz to 20.5 GHz for Model 585B, and in the range of 900 MHz to 26.7 GHz for Model 588B. The value entered by the user is truncated to 10 MHz resolution. This function is only available in Band 2. The frequency limit low must always be less than the frequency limit high. The number can be entered in any fixed-point format; the units terminator determines the scale of the input number.

Keyboard Examples:

PRESS: FREQ LIMIT LOW, CLEAR DATA to select the default value.

PRESS: FREQ LIMIT LOW, 2, ., 3, 5, GHz to select a 2.35 GHz value.

PRESS: FREQ LIMIT LOW, 3, 1, 3, 6, ., 3, MHz to select a 3130.0 MHz (3.13 GHz) value (truncated to 10 MHz resolution).

GPIB Example:

Enter: OUTPUT 718;"LOWLIMIT 2.356 GHZ" to select a 2.35 GHz value.

FREQ LIMIT HIGH

This key controls the high end of the frequency window that is searched for a signal in Band 2. Select the high frequency limit in the range of 900 MHz to 20.5 GHz for Model 585B, and in the range of 900 MHz to 26.5 GHz for Model 588B.

The value entered by the user is truncated to 10 MHz resolution. This function is only available in Band 2. Frequency limit low must always be less than frequency limit high.

The number can be entered in any fixed-point format; the units terminator determines the scale of the input number.

Keyboard Examples:

PRESS: FREQ LIMIT HIGH, CLEAR DATA to select the default value.

PRESS: FREQ LIMIT HIGH, 3 . 2 GHz to select a 3.2 GHz value.

PRESS: FREQ LIMIT HIGH, 2 1 0 9 8 MHz to select a 21,090 MHz (21.09 GHz) value (truncated to 10 MHz resolution).

GPIB Example:

Enter: OUTPUT 718;"HIGHLIMIT 3.2 GHZ" to selects a 3.2 GHz value.

CENTER FREQ

This key controls the center frequency mode of operation in which the counter looks for a signal in the vicinity of the CENTER FREQ value. This mode can be used to reduce the acquisition time or when measuring a particular signal in a multiple signal environment. This mode is available in Band 2 and Band 3.

Select Band 2 CENTER FREQ in the range of 950 MHz to 20 GHz for Model 585B, and in the range of 950 MHz to 26.5 GHz for Model 588B. The counter will lock onto signals within ±50 MHz from the entered value, depending on its power and frequency. The locking frequency is determined by the bandpass width of the YIG filter located at the input to Band 2.

Select Band 3 CENTER FREQ in the range of the subband currently selected. The counter will lock on signals ±1 GHz from the entered frequency. The counter will NOT reject signals outside this range. If a signal more than 1 GHz from the entered frequency is applied, an erroneous reading may result.

The value entered by the user is truncated to 10 MHz resolution. The number can be entered in any fixed-point format; the units terminator determines the scale of the input number.

Keyboard Examples:

PRESS: CENTER FREQ, CLEAR DATA to select the default value.

PRESS: CENTER FREQ, 1 4 . 8 GHz to select a center frequency value of 14.8 GHz.

PRESS: CENTER FREQ, 2 1 7 5 MHz to select a center frequency value of 2170 MHz (2.17 GHz, truncated to 10 MHz resolution).

GPIB Example:

Enter: OUTPUT 718;"CENTERFREQ 14.8 GHZ" to select a center frequency of 14.8 GHz.

SIGNAL MEASUREMENTS

AUTOMATIC FREQUENCY MEASUREMENTS

The EIP Models 585B and 588B Pulsed Microwave Frequency Counters can automatically measure the frequency of CW and repetitive pulse signals having pulse widths as narrow as 50 ns.

To measure the frequency of a CW signal, apply the signal to the input connector that corresponds to the frequency being measured and select the appropriate band. The counter then automatically finds the signal, measures it, and displays the measured frequency.

The average frequency of repetitive pulse signals is measured in much the same way as CW signals. The only difference is that for pulse signals with pulse recurrence frequencies of less than 2 kHz, the minimum pulse recurrence frequency must be entered into the counter using the MINPRF key on the front panel. If the MINPRF is not set at or below the minimum pulse repetition frequency of the signal to be measured, the counter will be unable to lock on the signal.

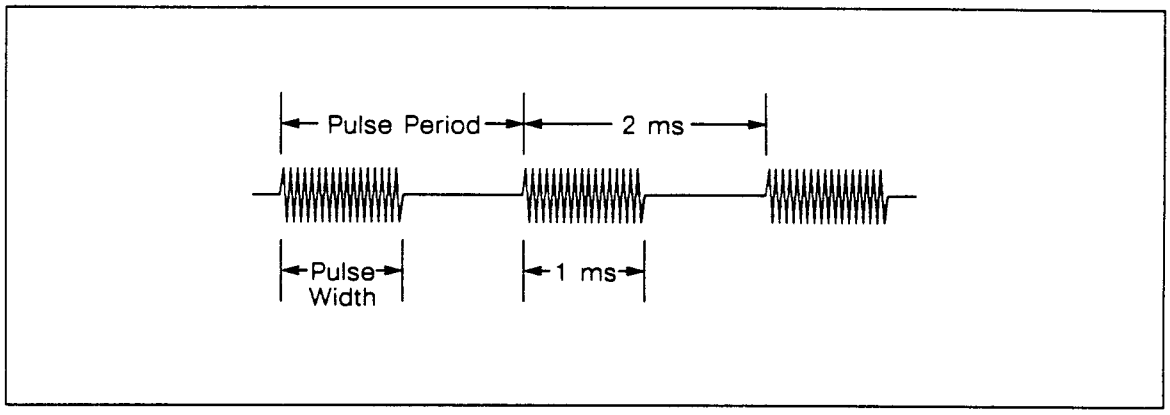

Figure 3-6. Pulsed Signal.

As an example, consider the signal shown in Figure 3-6. The signal is a 2 GHz signal with a pulse width of 1 ms and a pulse period of 2 ms. Since the pulse recurrence frequency is the recipical of pulse period, the minimum pulse repetition frequency of the signal shown is 500 Hz. Since this is less than 2 kHz, it must be entered into the counter. To enter a minimum pulse repetition frequency of 500 Hz into the counter, press the MIN PRF key followed by the 5 key, the 0 key, and the 0 key; then terminate the sequence with the Hz terminator key. If the signal at this point is applied to the Band 2 input connector and Band 2 is selected, the counter would automatically find the signal and display the frequency on the front panel.

These counters can also automatically measure both the pulse width and the pulse period of the incoming signal to a resolution of 10 ns. This is accomplished by pressing either the PULSE WIDTH key to measure the pulse width or the PULSE PERIOD key to measure the pulse period.

MULTIPLE SIGNAL MEASUREMENTS

In actual microwave environments, there are often multiple signals present. In a multisignal environment, the counter automatically finds and measures the largest signal (as specified by amplitude discrimination).

In Band 2, the counter can also measure signals other than the largest signal present. This is accomplished by setting frequency limits around the desired signal. Figure 3-7 shows an example of the frequency limits feature.

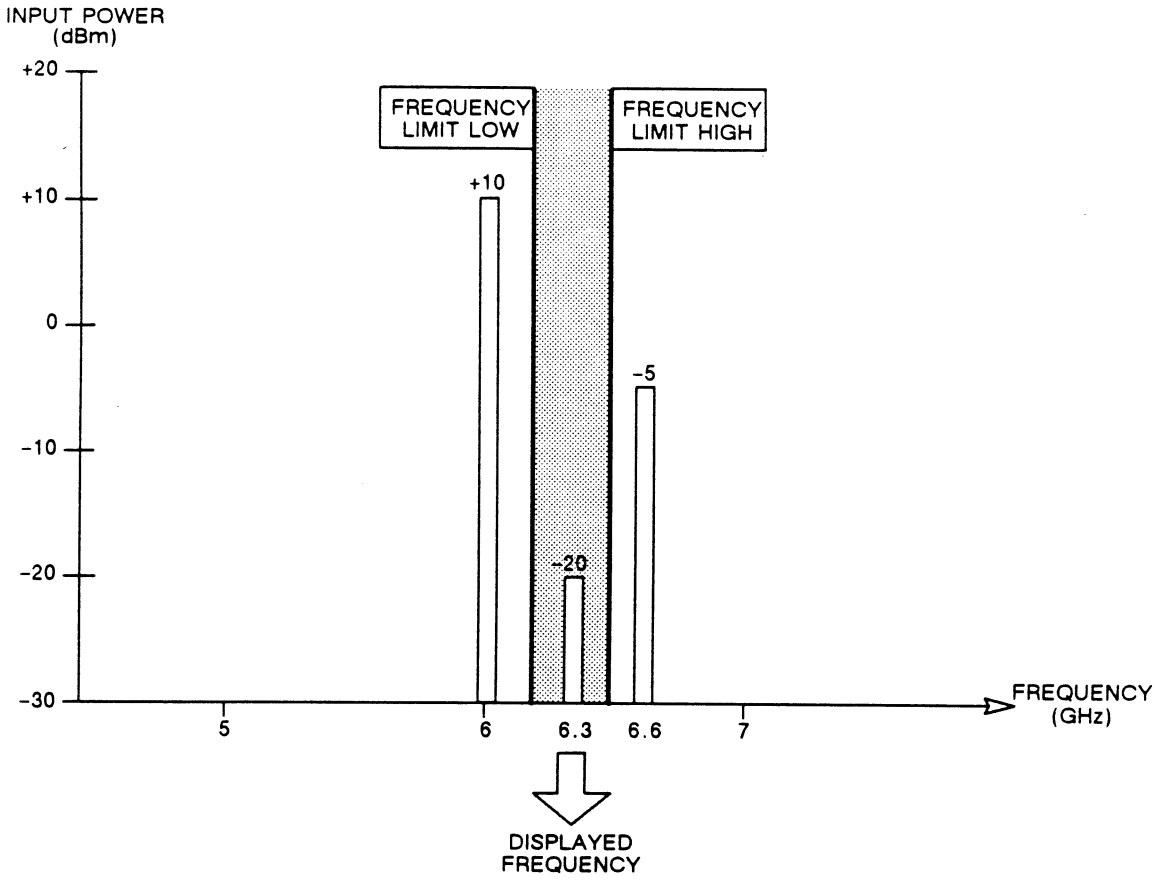

Figure 3-7. Frequency Limits.

If the signals shown in Figure 3-7 are applied to Band 2, the counter will automatically find the signal at 6 GHz since it is the largest signal. If it is desired to measure the signal at 6.3 GHz set the frequency limit low to 6.2 GHz and the frequency limit high to 6.4 GHz. This will prevent the counter from seeing either the signal at 6 GHz or the signal at 6.6 GHz.

The counter also provides a center frequency mode. In this mode, the counter automatically sets frequency limits around the specified center frequency. Referring back to Figure 3-7, the signal at 6.3 GHz could also be measured by entering a center frequency of 6.3 GHz. In the center frequency mode, the counter will lock on signals within 50 MHz of the specified center frequency.

PULSE PROFILING

Automatic pulse measurements determine the average frequency across a pulse. In some cases, however, additional information may be required. For example, a pulsed magnetron may exhibit substantial frequency shift near the leading and trailing edges of the pulse, or a pulsed Gunn diode oscillator may exhibit frequency shift during a pulse due to peak power thermal effects. Measurements of these characteristics are easily made using only the counter and a delaying pulse generator (See Figure 3-8).

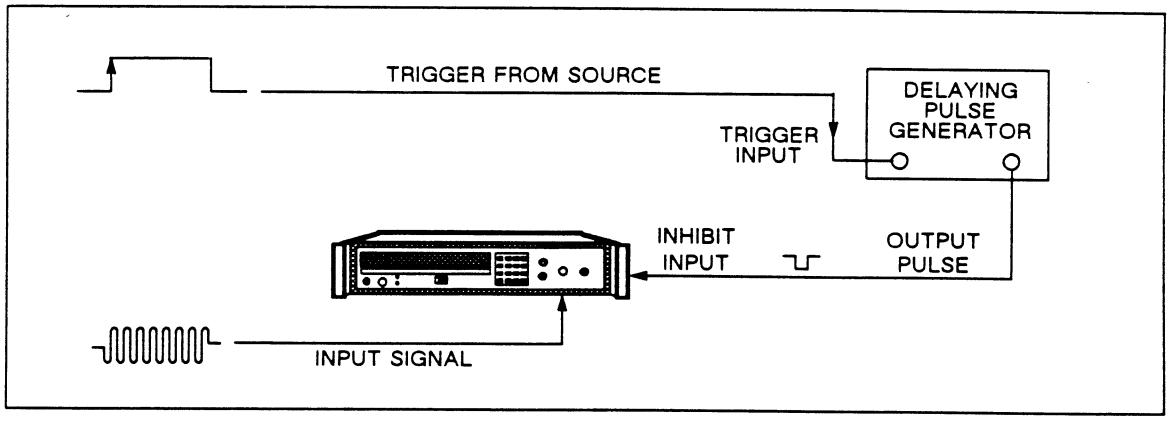

Figure 3-8. Pulse Profile Measurement Test Setup.

The output pulse of the signal generator is used as an enable input to the counter. As the pulse delay is varied, the measurement window can be "walked" through the pulse. A plot of frequency-versus-delay gives the frequency-versus-time profile of the pulse directly, as shown in Figure 3-9. The width of the measurement window is determined by the width of the pulse generator output. Measurement windows as narrow as 15 ns can be used, although wider windows yield higher accuracy.

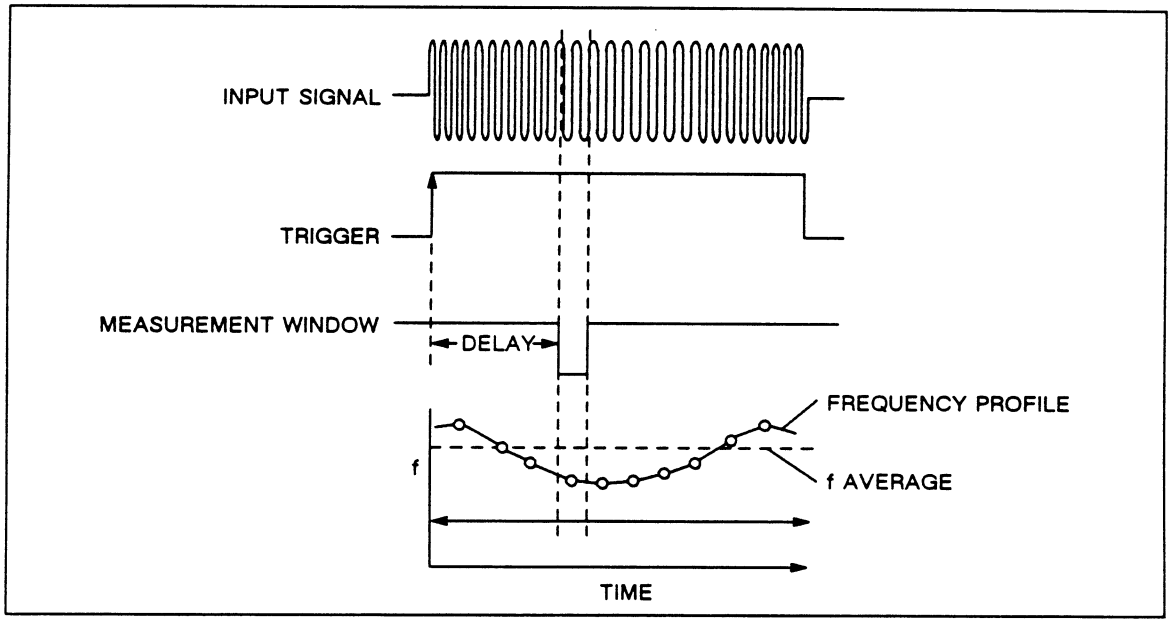

Figure 3-9. Pulse Profile Measurement.

VCO SETTLING TIME MEASUREMENTS

Many complex signals are not pulsed at all, but are continuous signals with frequencies that vary repetitively over time. One example is a settling time measurement of a voltage controlled oscillator (VCO). When a voltage step is applied to the tuning voltage input on a VCO its output frequency will change to reflect the voltage change on the tuning input. However, as shown in Figure 3-10, it takes the VCO a finite amount of time to settle in at the new frequency. The amount of time it takes for the VCO to settle in at the new frequency within some predetermined limits is specified as its settling time. A typical VCO settling time specification would require that the frequency output be within ±10 MHz of the settled frequency within 1 μs after the voltage step is applied to the tuning input on the VCO.

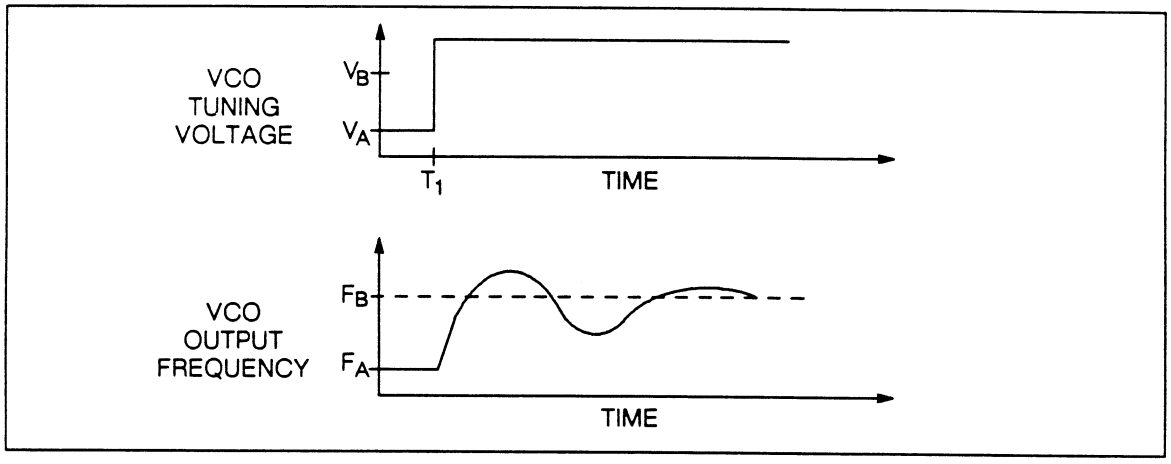

Figure 3-10. VCO Settling Time Measurements.

VCO settling time measurements can easily be made using the counter and a delaying pulse generator as shown in Figure 3-11.

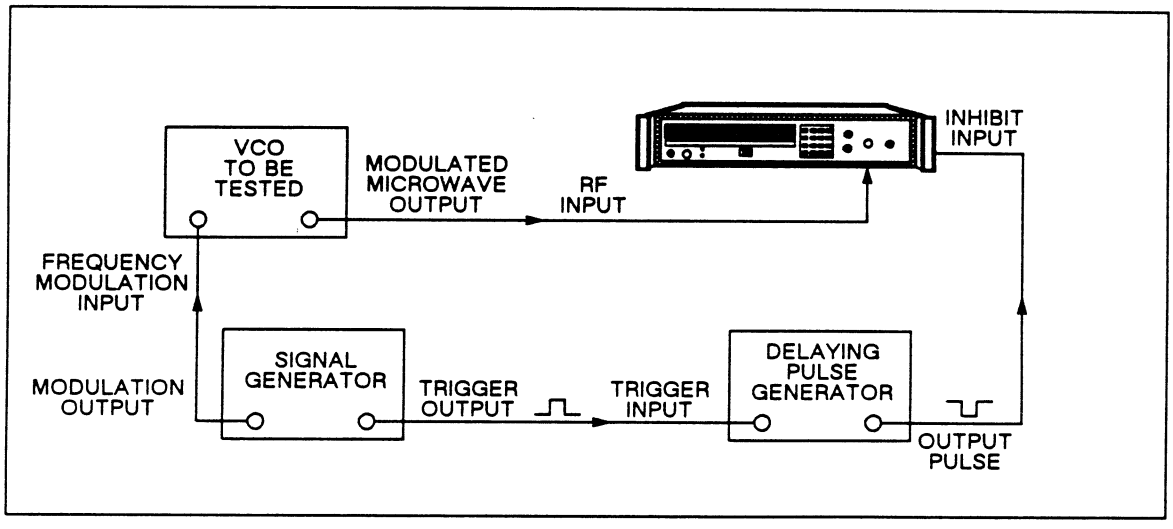

Figure 3-11. Time Varying Signal Measurement Test Setup.

FREQUENCY AGILE PULSE MEASUREMENTS

Another type of measurement is that of a repetitive sequence of pulses that differ in frequency. In this case, it is desirable to measure the frequency of each pulse in the sequence separately. The same test setup as shown in Figure 3-11 is required, with the trigger pulse synchronous with the sequence. In this measurement, the input inhibit is used to discriminate between pulses. The enabling pulse can be slightly wider than the pulse to be measured. By shifting the delay time of the enabling pulse, the user can measure each input pulse of the sequence separately.

TIMING CONSIDERATIONS

The internal timing usually should be of no concern to the user. However, in applications where a few nanoseconds are significant, two factors of internal operation must be considered. These involve two areas. One factor is the measurement window width, and the other is the internal timing delays.

Measurement Window Width

The measurement window width is the period during which the gate is actually open to enable the counting of a signal. This gate width will typically be 30 ns narrower than the pulse applied to the INHIBIT IN connector. The width of the gate is always an integral number of clock periods (12.5 ns). For applications where the measurement window must be known to an accuracy better than 20 ns, it is recommended that the gate output on the rear panel be observed on a high speed oscilloscope. The desired gate width may be set by varying the input inhibit pulse width. For accurate pulse representation, the oscilloscope input should be terminated in a 50 ohm load.

Internal Timing Delays

When it is necessary to measure the signal frequency at a precise point in time, the internal delays of the measuring instrument can be significant. In the EIP 585B and 588B counters, the total delay between the time a signal is applied to an input connector and the time it is available to be counted is nominally 60 ns. The signal threshold output on the rear panel typically occurs 20 ns after the signal is applied. The gate signal at the rear panel occurs at the measurement time with virtually no delay. In other words, when absolute time positioning of a signal is required, it is necessary to consider that the gate signal (representing the measurement period) is actually making a measurement of the signal which appeared at the input connector 60 ns earlier. If the signal threshold output is used as an indication of input signal, then it occurs 40 ns prior to measurement. Figure 3-12 shows the relative timing of these signals for a pulsed input signal. Timing, however, is not a function of input signal characteristics.

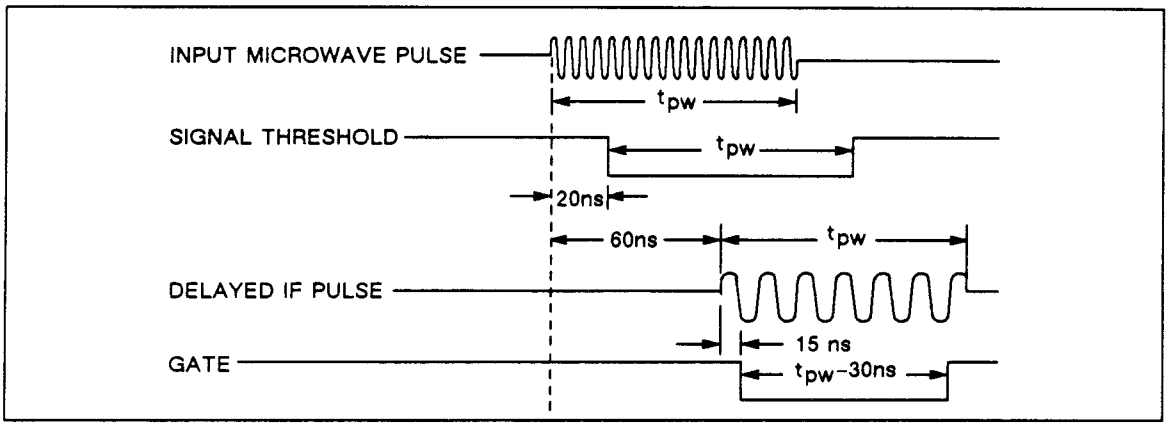

Figure 3-12. Internal Timing Delays.

ACCURACY

When making any type of measurement, some degree of measurement error exists. In EIP's CW type frequency counters, as with most other CW counters, these errors are limited to a combination of time base error, gate phasing error (±1 count), and gate width error. In making frequency measurements on pulsed RF signals, the preceding errors, along with one additional error due to distortion of the pulsed RF signal, affect measurement accuracy. To minimize these errors and to properly interpret the results of the measurements, the magnitude of these errors must be known.

CW MEASUREMENT ACCURACY

When measuring CW signals the measurement accuracy is specified as:

Total error = time base error ±1 count
(Based on measurement averaging)

Time base error causes an error in the measured frequency proportional to the error in the time base oscillator. For example, if the 10 MHz oscillator is off frequency by 3 Hz, the corresponding measurement error on a 1 GHz signal would be 300 Hz. For an 18 GHz signal, the same 3 Hz error in the time base would cause a measurement error of 5.4 kHz. The maximum error in the time base is the sum of the various possible errors, such as aging rate and temperature stability.

The second type of error, ±1 count, is due to the lack of phase coherence between the gate and the signal. Simply stated, if an event occurs every 400 ms (F = 2.5 Hz), a counter could measure either 2 or 3 events in a one second interval.

The above note "based on measurement averaging" is included due to a random instrumentation error in the counter. This error can be virtually eliminated by averaging measurements.

PULSE MEASUREMENT ACCURACY

Each of the sources of CW measurement error contribute to the overall error in pulsed frequency measurements, along with gate error and distortion error. For narrow pulses, the averaging error and gate error can become the dominant sources of error for pulse measurements. The following list describes the source of potential measurement errors when using the EIP 585B and 588B counters.

Time Base Error

A frequency error in the time base reference oscillator results in a proportional frequency measurement error. Two main sources of time base error are aging rate and temperature stability. Aging rates of less than 1×10^{-7} parts per month, and temperature stability of 1×10^{-6} over the range of 0 to 50 °C, are standard on the 585B and 588B counters.

SAMPLE ERROR CALCULATIONS

Following are sample calculations for determining the measurement error of the counter, based on the time base aging rate.

Given: Aging rate: 1×10^{-7}/month
Calibration interval: 6 months
Frequency: 20 GHz

Calculation: Error $= \pm$(aging rate x cal. interval x frequency)

$$= \pm\left(\frac{1 \times 10^{-7}}{\text{mo.}} \times 6 \text{ mo.} \times 2 \times 10^{10} \text{ Hz}\right)$$

$$= \pm(6 \times 10^{-7} \times 2 \times 10^{10} \text{ Hz})$$

$$= \pm(12 \times 10^{3} \text{ Hz})$$

$$= \pm 12 \text{ kHz}$$

Counter measurement, after a six-month calibration interval, could have an error of $\pm$12 kHz in measuring a 20 GHz signal.

Given: Aging rate: 1×10^{-7}/month
Calibration interval: 12 months
Frequency: 20 GHz

Calculation: Error $= \pm$(aging rate x cal. interval x frequency)

$$= \pm\left(\frac{1 \times 10^{-7}}{\text{mo.}} \times 12 \text{ mo.} \times 2 \times 10^{10} \text{ Hz}\right)$$

$$= \pm(12 \times 10^{-7} \times 2 \times 10^{10} \text{ Hz})$$

$$= \pm(24 \times 10^{3} \text{ Hz})$$

$$= \pm 24 \text{ kHz}$$

Counter measurement after the recommended 12-month calibration interval could have an error of $\pm$24 kHz in measuring a 20 GHz signal just due to time base aging.

These examples are to illustrate error due to the time base aging rate only. Actual calculations of measurement error must include the other sources of error discussed in the following text.

Averaging Error

This error is caused by the relative timing between the gate and the incoming signal and results in an uncertainty of $\pm$1 count in the least significant digit of each measurement. If the counter resolution is set to 10 kHz, then the potential error is $\pm$10 kHz. On signals having pulse widths less than the required gate time (determined by the resolution), the counter will generate more than one gate per measurement cycle. If the counter generates N number of gates, then an uncertainty of $\pm$N counts is possible though very unlikely. The resultant averaged measurement follows the rules of statistics in that, on successive gates, the $\pm$1 count error will vary randomly to a certain degree. In fact, most of the readings (63%) will fall between $\pm$ the square root of N, where N is the number of gates required to accumulate the required gate time. This is called the RMS averaging error. In the following formulas, N = RES/GW. It should be noted that the total gate time is typically 30 ns narrower than the input pulse. The RMS averaging error, in Hz, can be calculated by using the following formulas:

Bands 1 and 3: averaging error (RMS) $= \pm 2\sqrt{\text{RES/GW}}$

Band 2 : averaging error (RMS) $= \pm\sqrt{\text{RES/GW}}$

Where: RES is the specified instrument resolution in Hz, up to 1 MHz. Above 1 MHz, RES is always 1 MHz. GW is the logical AND of the pulse width and the inhibit signal minus 30 ns. See Figure 3-13 for a graphical description of the logical AND function.

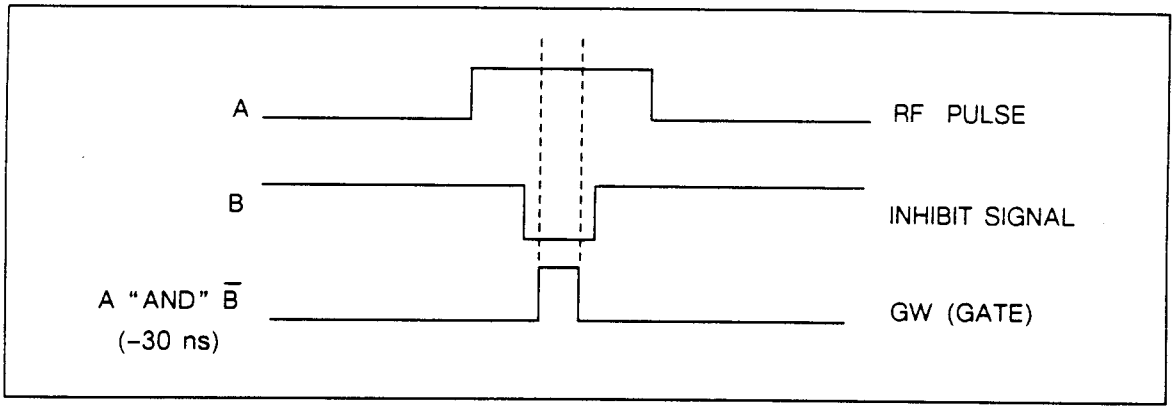

Figure 3-13. Logical "AND" Function.

Gate Error

When narrow pulses are counted, the gate is opened and closed many times in order to accumulate enough gate time to provide the required resolution. Each time the gate opens and closes, there will be a small but finite error. The total error is proportional to the number of times the gate is cycled during a measurement, and is inversely proportional to the gate width. This error is also related to both temperature and input frequency. In the 585B and 588B counters, the worst case gate error, including all variables, is specified as:

Band 1: gate error = $\pm 0.07/GW$

Band 2: gate error = $\pm 0.01/GW$

Band 3: gate error = $\pm 0.03/GW$

Where: GW, in seconds, is the logical AND of the pulse width and the inhibit signal minus 30 ns. Unlike averaging error, which is random, gate error is systematic, and is not reduced by averaging.

Distortion Error

During the first and last few nanoseconds of a pulse, phase distortion caused by impedance mismatches or video effects can occur, resulting in shifts in time of the zero crossing. On wide pulses, distortion error is insignificant; however, on narrow pulses it may become the dominant source of error. To reduce the effect of distortion error on count accuracy, the 585B and 588B counters automatically adjust the gate to start 15 ns after the pulse begins, and to end 15 ns before the end of the pulse. The specified maximum distortion error for all three bands can be calculated from the following formula:

$$\text{Maximum Distortion Error} = \pm 0.03/(PW - 30\text{ ns})$$

Where: PW = pulse width (minimum pulse width is 50 ns)

TECHNIQUES FOR IMPROVING ACCURACY

In most cases, the specified counter accuracy will be more than sufficient to meet measurement requirements. If greater accuracy is required, all four sources of error can be minimized by a combination of calibration, long term averaging, added correction factors, and signal conditioning.

TIME BASE CALIBRATION

A frequency error in the internal time base oscillator results in a proportional error in the frequency reading for either CW or pulsed signals. The aging rate of the internal time base is specified to be less than 1×10^{-7} parts per month. This means that if the oscillator were set precisely on frequency at the beginning of the month, it could be 1 Hz off frequency at the end of the month. On a frequency measurement of 18 GHz, a 1 Hz error in the 10 MHz time base would cause a measurement error of 1.8 kHz. Other errors can result from changes in ambient temperature. Measurement errors caused by the time base can be reduced by adjusting the time base at the temperature it will be used using a standard of known accuracy. Another error reduction method is to use an external 10 MHz time base with a known degree of accuracy, such as an oven oscillator, or a 10 MHz frequency standard.

REDUCING AVERAGING ERROR

Averaging error is reduced to ± 1 count whenever the gate width (GW) is greater than 1/RES where RES is the counter resolution in Hz. Since the averaging error is random in nature, it can also be reduced by increasing the number of individual gates. This can be accomplished by increasing the resolution of the counter and/or averaging a number of individual measurements. The counter allows 1 kHz maximum resolution and can automatically average up to 99 individual measurements internally. With the GPIB and a controller, the user can average a larger number of individual measurements, which will virtually eliminate averaging error. The following formulas can be used to determine the averaging error (RMS) when averaging a number of individual measurements.

$$\text{Bands 1 and 3: averaging error (RMS)} = \pm 2\sqrt{\text{RES}/[(\text{GW})(\text{AVG})]}$$

$$\text{Band 2 : averaging error (RMS)} = \pm\sqrt{\text{RES}/[(\text{GW})(\text{AVG})]}$$

Where: RES is the specified instrument resolution in Hz, up to 1 MHz. Above 1 MHz, RES is always 1 MHz. GW is the logical AND of the pulse width and the inhibit signal minus 30 ns. AVG is the number of individual measurements to be averaged.

REDUCING GATE ERROR

Gate error at any given frequency and pulse width can also be virtually eliminated by comparing a CW frequency measurement to a simulated pulsed frequency measurement and computing a correction factor due to gate error. This correction factor can then be added to, or subtracted from, the indicated pulsed measurement to obtain the corrected frequency. The CW signal should be the same frequency (within 25 MHz) as that of the actual pulsed signal to be measured. To simulate a pulsed signal, apply an enable signal (of the same width as the pulse to be measured) to the INHIBIT IN connector on the rear panel. A single measurement will contain both averaging error and gate error. Averaging measurements will reduce averaging error by the square root of the number of measurements averaged. If 100 measurements are averaged, the averaging error will be reduced by a factor of 10. Gate error, and any residual averaging error, is the difference in reading between the pulsed and nonpulsed measurement of the same CW signal.

Example: Pulse frequency = 2 GHz
Pulse width = 2 μs

1. Apply a CW signal to the counter at 2 GHz ±25 MHz and record the displayed frequency. This frequency will be called F1.

2. Apply an ECL signal with a pulse width of 2 μs at the INHIBIT IN connector on the rear panel. Set the counter to average 99 readings. The frequency displayed on the counter will be called F2.

3. Gate Error = F2 – F1

NOTE

This procedure avoids errors associated with pulsed signal distortion and any possible pulling of the signal source. It should be noted that by using Special Function 92, gate error can also be automatically calibrated out of the system for a given pulse width and frequency. However, the calibration procedure may result in additional errors for other pulse widths or frequencies. For additional information on Special Function 92, see the service manual.

REDUCING DISTORTION ERROR

Since distortion error is most significant on the edges of the pulse, it may be reduced by using the counter inhibit feature to measure only in the middle of the pulse; however, measuring only the middle of the pulse narrows the gate, and gate error will increase. For pulses less than 70 to 80 ns, this may add more error than it removes. The performance test section of the service manual describes a method of determining the magnitude of this error that can be used to determine the improvement in accuracy achieved by using the inhibit function.

CALCULATING MEASUREMENT ACCURACY

Following is a sample calculation for determining the maximum specified measurement error for a typical pulse frequency measurement.

Given: Frequency: 18 GHz
Pulse width: 530 ns
Resolution: 100 kHz

- TIME BASE ERROR (TBE) (Based on 6 Hz error from 10 MHz time base) – – – – ±10.8 kHz

  TBE = (6 Hz/10 MHz)(18 GHz) = 10.8 kHz

NOTE

The direction of the time base error is not specified, so it is not known whether the time base error caused the indicated reading to be higher or lower. If the actual frequency of the time base was 6 Hz high, then its period would be reduced and the counter would indicate a lower frequency.

- RMS AVERAGING ERROR (AE) - ±45 kHz

  $AE\ (RMS) = \pm\sqrt{RES/[(GW)(AVG)]}$

  Where: RES = specified counter resolution
  GW = (pulse width AND inhibit signal) - 30 ns
  AVG = number of measurements averaged

  $AE\ (RMS) = \pm\sqrt{(100E3)/(500E-9)(99)} = \pm 45$ kHz

NOTE

To reduce the averaging error for this example, the measurement averaging feature of the counter was used. If it had not been used, the averaging error would have been ±450 kHz.

- GATE ERROR (GE) (Worst Case) - ±20 kHz

  $GE = \pm 0.01/GW$

  Where: GW = (pulse width AND inhibit signal) - 30 ns

  $GE = \pm 0.01/500E-9 = \pm 20$ kHz

- DISTORTION ERROR (DE) (Worst Case) - ±60 kHz

  $DE = \pm 0.03/(PW - 30\ ns)$

  Where: PW = pulse width

  $DE = \pm 0.03/(530\ ns - 30\ ns) = \pm 60$ kHz

- **TOTAL ERROR** = SUM OF INDIVIDUAL ERRORS - - - - - - - - - - - - - - - - - - ±136 kHz

NOTE

The total measurement error, as calculated above, is the worst case error. The errors that make up the total error would not under normal circumstances be additive. Errors in opposite directions would offset one another, with the effect of reducing the total error.

MEASUREMENT ACCURACY WORKSHEET

The following worksheet can be used to determine the maximum specified measurement error for a particular application. To determine the specified maximum error, select the desired operating parameters and use the formulas given to determine the magnitude of each type of error.

VARIABLES: Frequency (F): _____

Pulse width (PW): _____

Counter resolution (RES): _____

SUM INDIVIDUAL ERRORS

- TIME BASE ERROR

  This error can be determined by accurately measuring the frequency at the rear panel 10 MHz IN/OUT connector. The frequency measured (F mea) is then used in the following formula to determine measurement error.

  TBE = ((10 MHz - F mea)/10 MHz)(F) _____

  Where: F mea = measured time base frequency

  F = input frequency

- RMS AVERAGING ERROR

  Bands 1 and 3: AE (RMS) = $\pm 2\sqrt{RES/[(GW)(AVG)]}$ _____

  Band 2 : AE (RMS) = $\pm\sqrt{RES/[(GW)(AVG)]}$ _____

  Where: RES = specified counter resolution in Hz up to 1 MHz. Above 1 MHz resolution, the counter's internal resolution remains at 1 MHz.
  GW = (pulse width AND inhibit signal) - 30 ns
  AVG = number of measurements averaged

  NOTE

  If GW is > 1/RES then AE = ±1 count

- GATE ERROR (Worst Case)

  Band 1: GE = ±0.07/GW _____

  Band 2: GE = ±0.01/GW _____

  Band 3: GE = ±0.03/GW _____

  Where: GW = (pulse width AND inhibit signal) - 30 ns

- DISTORTION ERROR (Worst Case)

  DE = ±0.03/(PW - 30 ns) _____

  Where: PW = pulse width

TOTAL ERROR = sum of individual errors _____

SPECIAL FUNCTION DIRECTORY

Counter special functions can be divided into three categories:

1. Counter operation verification
2. Calibration/troubleshooting aids
3. Counter capability enhancements

The special functions are grouped according to the above categories. Further information about how each one works is summarized at the end of each discussion. The summary covers the following features:

- ONE-SHOT OR CONTINUOUS ACTION

  One-shot action functions - automatically revert the counter to its normal operation after a specific action has been taken. These special functions are designated ONE-SHOT.

  Continuous action functions - supersede all normal operations of the counter and cause it to stay in the special function mode until the user terminates the function. Most continuous action functions can be terminated by pressing any key on the keyboard or entering any function command through the GPIB interface. After the special function is terminated, the function corresponding to the key pressed or the command entered will be serviced and a reset will be generated. Exceptions to the above termination sequence will be stated in the individual special function descriptions. These functions are designated STOP/RESET or STOP/NO RESET as applicable.

- SPECIAL FUNCTION (SPC) INDICATOR ON OR OFF: at the end of a special function description, this indicates whether the SPC status indicator on the front panel is on or off upon exiting the special function.

- SPECIAL STATUS BIT (SB) ON OR OFF: indicates whether the special on/off bit in the status byte is on or off during the special function.

ACTIVATION OF SPECIAL FUNCTIONS

CAUTION

Executing Special Function 46, 76, 91, or 92 can cause a loss of calibration data. To prevent this from occurring, access to these functions is blocked by an internal memory protect feature. Attempting to access these functions with the memory protected will cause the counter to display "ERROR 53". Refer to section 7 for information on unprotecting the memory.

Special functions can be activated through both the front panel keyboard and the GPIB interface. To activate a special function through the keyboard, press the SPECIAL key followed by two digit keys. To activate a special function through the GPIB interface, enter the word SPECIAL followed by a two-digit number. Activating special functions will not alter any previously entered parameters unless specifically stated. To terminate all previously activated special functions: press the SPECIAL key and then the 0 key followed by the 0 key again; or, press the SPECIAL key followed by the CLEAR DATA key. To terminate all special functions using GPIB, issue the command SPECIAL 00.

OPERATION VERIFICATION FUNCTIONS

Special Functions numbered 01 through 09 provide the user with a means of verifying that the counter is operational.

SPECIAL FUNCTION 01 --- 100 MHz Self Test

This function verifies that the count chain, gate generator, and VCO are operational.

When this function is entered, the counter:

1. Exits the current band
2. Sets the hardware to the self-test mode
3. Sets the VCO to 400 MHz
4. Sets the counter to take frequency measurements only
5. Starts measurement cycles

The display shows the frequency measurement results. These results are output to the GPIB interface when frequency readings are requested. The measurement result should be 100 MHz ±1 count.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 02 --- Light Display Segments Test

This function verifies that all the digit segments and annunciator LEDs are operational. When this function is activated, all digit segments and all annunciators will be turned on. The GATE and the SEARCH annunciators will both be on for the duration of the special function.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 03 --- Scan Display Segments Test

Each segment in all the digits and banks of annunciators is turned on sequentially by this function to test the display segment drivers. The scan rate is determined by the setting of the SAMPLE RATE control.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 04 --- Scan Display Digits Test

Each digit and each bank of annunciators is turned on sequentially by this function to check the display digit driver. The scan rate is determined by the setting of the SAMPLE RATE control.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 05 --- Keyboard Test

This function verifies the operation of the keyboard.

After this function is activated the counter stops normal operations and the display shows the key code of the last key pressed. When a new key is pressed, the display is updated to show the code of the new key. When the GPIB controller requests a key code, the code of the last key pressed is output. (If the controller requests a key code, the counter outputs to the GPIB interface the code of the last key pressed even if Special Function 05 is not activated). If the

counter is in LOCAL, this function must be terminated by the CLEAR DISPLAY key. If it is in remote, this function can be terminated by any device-dependent command

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 06 — PROM Check Sum Test

This function generates the check sum for each PROM in the counter and compares it with the check sum table stored in the firmware. If all the check sums generated are correct, the counter displays the word "PASSEd" on the front panel. If any one of the check sums is incorrect, an error message corresponding to that particular check sum is output to the display. At the same time, the error condition status bit in the GPIB serial poll status byte will be set. During check sum generation, "SPECIAL 06" is displayed.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 07 — Display Counter Model Number

This function enables the user to find out whether the counter is configured as a 585B or 588B counter. After the appropriate model number is displayed on the front panel, the counter returns to the measurement mode. No reset is generated.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 08 — External Timebase Select

Selecting this function configures the counter to external timebase input mode.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:ON

SPECIAL FUNCTION 09 — Internal Timebase Select

Selecting this function configures the counter to internal timebase mode.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:ON

CALIBRATION AND TROUBLESHOOTING FUNCTIONS

Special Functions number 20, 40-42, 44-47, 91, and 92 aid the user in calibrating and/or troubleshooting the counter.

SPECIAL FUNCTION 20 — Band 2 Detected RF Level

This function verifies coarse calibration of the Band 2 YIG DAC offset and YIG DAC slope adjustments.

When this function is activated, the counter waits for the user to enter the new YIG calibration frequency. The previously entered frequency number and "Fr" are displayed in the frequency section and the pulse parameter section of the display, respectively. The special function stops in this state until the user enters a new frequency number; or, if the previously entered frequency number is the required frequency, the kHz key can be pushed to tell the special function to continue.

After the number has been entered, the YIG DAC is set to the entered frequency number. The display shows "CAL dAC" plus a number from 1 to 8 that corresponds to the information on the Band 2 power discrimination circuitry. The counter will output the power discrimination circuitry information when requested by the GPIB to output LEVEL. (For more calibration information, see Section 7.)

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 40 — Sweep YIG DAC

When this function is activated, the counter waits for the user to enter the start frequency of the YIG sweep. The previously entered start frequency and "F1" are displayed in the frequency section and the pulse parameter section of the display, respectively. The special function stops in this state until the user enters a new start frequency or, if the previously entered frequency is the required start frequency, the user presses the kHz key to tell the special function to continue.

After the start frequency is entered, the counter waits for the user to enter the stop frequency of the YIG sweep. The previously entered stop frequency and "F2" are displayed in the frequency section and the pulse parameter section of the display, respectively. The special function will stop in this state until the user enters a new stop frequency or, if the previously entered frequency is the required stop frequency, the user presses the kHz key to tell the special function to continue.

When both the start and stop frequencies have been entered, the display reverts to displaying "SPECIAL 40". In CCN 6804 (585B) and CCNs 6905 and 6906 (588B) models, the YIG DAC sweeps continuously from F1 to F2 in 2 MHz steps until the function is terminated. In CCN 6805 (585B) and 6907 (588B) models, the YIG DAC sweeps continuously from F1 to F2 in steps determined by the difference between the low and high sweep limit (Step Size = [High - Low]/512) until the function is terminated. The minimum step size is 2 MHz. In all models, the sweep rate is controlled by the setting of the SAMPLE RATE control. Maximum sweep rate may be obtained by disabling the sample rate (Special Function 63) before calling this function. If F1 and F2 are equal, the YIG DAC will be set to the frequency corresponding to F1 and F2.

To activate this function in remote, the user programs the controller to output SPECIAL 40. The start and stop frequencies used will be the frequencies specified in the GPIB commands Y1FREQ and Y2FREQ (where Y1FREQ and Y2FREQ correspond to F1 and F2 respectively). If the start or stop frequency required is different from that specified in Y1FREQ or Y2FREQ respectively, the number in that frequency register must be updated before Special Function 40 is activated.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 41 — Sweep VCO with VCO Power Amplifier On

After this function is activated, the counter waits for the user to enter the start frequency of the VCO sweep. The previously entered start frequency and "F1" are displayed in the frequency section and the pulse parameter section of the display, respectively. The special function will stop in this state until the user enters a new start frequency or, if the previously entered frequency is the required start frequency, the user presses the kHz key to tell the special function to continue.

After the start frequency is entered, the counter waits for the user to enter the stop frequency of the VCO sweep. The previously entered stop frequency and "F2" will be displayed in the frequency section and the pulse parameter section of the display, respectively. The special function will stop in this state until the user enters a new stop frequency or, if the previously entered frequency is the required stop frequency, the user presses the kHz key to tell the special function to continue.

When both the start and stop frequencies have been entered, the display will revert to displaying "SPECIAL 41". The VCO sweeps continuously from F1 to F2 in 50 kHz steps until the function is terminated. The sweep rate is controlled by the sample rate. Maximum sweep rate may be obtained by disabling the sample rate (Special Function 63) before calling this function. If F1 and F2 are equal, the VCO will be set to that particular frequency. The VCO power amplifier is turned on during this function.

To activate this function in remote, the user instructs the controller to output SPECIAL 41. The start and stop frequencies used will be the frequencies specified in the GPIB commands V1FREQ and V2FREQ (where V1FREQ and V2FREQ correspond to F1 and F2 respectively). If the start or stop frequency required is different from that specified in V1FREQ or V2FREQ, the number in that frequency register must be updated before SPECIAL 41 is activated.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 42 --- Sweep VCO with VCO Power Amplifier Off

After this function is activated, the counter will wait for the user to enter the start frequency of the VCO sweep. The previously entered start frequency and "F1" will be displayed in the frequency section and the pulse parameter section of the display, respectively. The special function will stop in this state until the user enters a new start frequency or, if the previously entered frequency is the required start frequency, the user presses the kHz key to tell the special function to continue.

After the start frequency is entered, the counter will wait for the user to enter the stop frequency of the VCO sweep. The previously entered stop frequency and "F2" will be displayed in the frequency section and the pulse parameter section of the display respectively. The special function will stop in this state until the user enters a new stop frequency or, if the previously entered frequency is the required stop frequency, the user presses the kHz key to tell the special function to continue.

When both the start and stop frequencies have been entered, the display will revert to displaying "SPECIAL 42". The VCO sweeps continuously from F1 to F2 in 100 kHz steps until the function is terminated. The sweep rate is controlled by the sample rate Maximum sweep rate may be obtained by disabling the sample rate (Special Function 63) before calling this function. If F1 and F2 are equal, the VCO will be set to that particular frequency. The VCO power amplifier is turned off during this function.

To activate this function in remote, the user instructs the controller to output SPECIAL 42. The start and stop frequencies used will be the frequencies specified in the GPIB commands V1FREQ and V2FREQ (where V1FREQ and V2FREQ correspond to F1 and F2, respectively). If the start or stop frequency required is different from that specified in V1FREQ or V2FREQ, the number in that frequency register must be updated before SPECIAL 42 is activated.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 44 --- Disable Normal Operations

This function prevents the counter from performing the normal converter lock and measurement cycles. It freezes the counter in the state it was in at the moment the function was activated. The display will show "PAUSE" and the STOP ON/OFF status bit will be set when this function is active. Special Function 44 remains activated until terminated through Special Function 45 or by pressing the SPECIAL key followed by the CLEAR DATA key, or by pressing the SPECIAL key followed by the 0 key and then the 0 key again.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 45 --- Enable Normal Operations

This function reverses the action taken when Special Function 44 is activated. The function returns the counter to normal operation. A reset is generated and the STOP ON/OFF status bit is cleared when this function is activated.

STOP/RESET SPC INDICATOR:OFF SPECIAL SB:ON

SPECIAL FUNCTION 46 --- Display and/or Alter Memory

CAUTION

Care must be used when operating Special Function 46. Although the counter cannot be damaged by this function, stored calibration data can be changed. For this reason, access to this function is blocked by an internal memory protect feature. Attempting to access this function with the memory protected will cause the counter to display "ERROR 53". Refer to section 7 for information on unprotecting the memory.

This function allows the user to display and/or alter any memory location. The counter continues its normal operations when performing this function unless Special Function 44 has previously been activated.

In the local mode, the keys on the keyboard take on different meanings after Special Function 46 is activated. Following are the definitions of the keys when the counter is in this function.

- All number keys remain number keys.
- GHz key = hexadecimal digit A
- MHz key = hexadecimal digit B
- kHz key = hexadecimal digit C
- Hz key = hexadecimal digit D
- . key = hexadecimal digit E
- ± key = hexadecimal digit F
- PULSE WIDTH key = INCREMENT command.
- PULSE PERIOD key = DECREMENT command.
- CLEAR DATA key = ADDRESS command.
- CLEAR DISPLAY and INIT keys remain the same.

After activating Special Function 46, the user can do one of the following:

- Exit the function by issuing a CLEAR DISPLAY command (pressing the CLEAR DISPLAY key).
- Alter the content of the memory location by entering a two-digit hexadecimal number.
- Display the next memory location by issuing an INCREMENT command (pressing the PULSE WIDTH key).

- Enter another memory address by first issuing an ADDRESS command (pressing the CLEAR DATA key).

If the content of a memory location is altered, the new content of that memory location is displayed in the pulse parameter section of the display. If the ADDRESS command is issued, the display will change to show "Addr_ _ _ _". While the address is being entered, the hexadecimal digits keyed in replace each blank sequentially. After the memory address is entered, the content of that memory location is displayed in the pulse parameter section of the display. This function must be terminated by the CLEAR DISPLAY command.

In the remote mode, a memory content can be interrogated by using the OUTPUT MEMORY command. When the counter is addressed to talk, the last memory address accessed will be output. A memory location can be accessed using the MEMORY 0HHHH command (where H is a hexadecimal digit). The content of a memory location can be altered using the MEMORY 0HHHH 0HH command. In the remote mode, Special Function 46 need not be activated when accessing and altering memory locations. Those operations can be done by the controller in the background.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 47 --- Measure IF Only

This function provides the user with the means to measure the frequency of the IF signal, present at the input of the count chain assembly, without having the counter converter locked on the signal. The counter will not measure pulse parameters when this function is activated.

When Special Function 47 is activated, the counter stops the normal converter lock and measurement cycles. The VCO, YIG, and all microprocessor-controlled hardware switches are left at the state they were in when the function was activated. The counter then starts measuring the frequency of the IF signal present at the input to the count chain assembly. The measurement results are displayed on the front panel and are also output via the GPIB interface if frequency readings are requested. Note: This function does not check periodically for the presence of a signal as in the normal operation of the counter.

STOP/RESET SPC INDICATOR:ON SPECIAL SB:ON

CAPABILITY ENHANCEMENT FUNCTIONS

Special functions number 61-71, 72-76, and 90 provide, to sophisticated users, those functions that are not required in the normal use of the counter.

SPECIAL FUNCTION 61 --- Disable Input Signal Tracking

This function configures the counter to skip the execution of the input signal tracking function that normally occurs after every measurement cycle. This function shortens the measurement cycle time, but prohibits the counter from tracking a moving signal.

The action taken with this function can be reversed by activating Special Function 62.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 62 --- Enable Input Signal Tracking

This function allows the user to reverse the action taken with Special Function 61.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 63 --- Disable Sample Rate Control

This function configures the counter to ignore the local and the remote sample rate controls. The counter measurement cycle rate is maximized, which shortens the measurement cycle time.

The action taken with this function can be reversed by activating Special Function 64.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 64 --- Enable Sample Rate Control

This function allows the user to reverse the action taken with Special Function 63.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 65 --- Disable Results Display

This function prohibits the output of measurement results to the front panel display. When Special Function 65 is activated, the front panel displays only a row of dots. When the user enters parameters through the keyboard, the display responds normally. This function shortens the measurement cycle time and provides security in systems used with classified frequencies.

The action taken with this function can be reversed by activating Special Function 66.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 66 --- Enable Results Display

This function is used to reverse the action taken by Special Function 65. When this function is activated, the display is immediately updated with the last measurement results.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 67 --- Display Pulse Repetition Frequency (PRF)

This function configures the counter to display the pulse period measurements as a frequency. It has no effect on pulse width measurements.

After this function is turned on, frequency measurements will NOT be displayed on the front panel. The pulse period will be displayed to the maximum available resolution, using the pulse parameter display as the 100 Hz, 10 Hz and 1 Hz digits. Since the PRF is derived mathematically from the period, the resolution will be a function of the period measurement resolution per the formula:

$$\text{Resolution (Hz)} = \frac{1}{\text{Period} \pm 10\text{ns}} - \frac{1}{\text{Period}}$$

When requested by the GPIB bus controller to output a period measurement, the counter outputs a frequency corresponding to the PRF of the input signal.

If pulse period measurements are enabled, Special Function 67 has a higher priority than Special Function 69. That is, the front panel will be configured according to Special Function 67 if both Special Function 67 and Special Function 69 are activated.

This function is terminated when Special Function 68 is activated.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 68 --- Display Pulse Period

This function allows the user to reverse the action taken with Special Function 67.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 69 --- Display Pulse Parameter Measurements Only

When this function is activated, frequency measurements are not displayed on the front panel. Instead, the 12 digits on the front panel are devoted exclusively to displaying pulse parameter measurements to 10 ns resolution.

If the pulse period function is on, this special function has a lower priority than Special Function 67. That is, the front panel is configured according to Special Function 67 if both Special Function 67 and Special Function 69 are activated.

This function is terminated when Special Function 70 is activated.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 70 --- Display Frequency and Pulse Parameter Measurement

This function returns the counter to the normal mode of displaying measurement results, reversing the action taken by Special Function 69.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 72 --- Store Counter Setup and/or Default Values

This function serves two purposes. Its primary use is to store the present counter setup in the storage register specified. When this function is activated, the counter requests the user to enter the register number by displaying "REG _" on the front panel. The counter remains in this state until the user enters a number between 0 and 9. After the register number is entered, the function stores the current counter setup in the register specified. During this time, "REG N" is displayed on the front panel (where N is the register number entered).

This function also can be used to customize the default values used by the counter. The default values determine the state of the instrument at turn-on. This is accomplished by setting the instrument up in the desired turn-on condition and storing it in register 0. The information stored in register 0 is used to determine the power-on state of the counter. To clear the instrument back to the factory-set default values, select Special Function 72 and press the CLEAR DATA key.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 73 --- Recall Counter Setup

This function recalls the counter setup stored in the storage register specified.

When this function is activated, the counter requests the user to enter the register number by displaying "REG _" on the front panel. The counter remains in this state until the user enters a number between 0 and 9. After the register number is entered, the function proceeds to set up the counter according to the information stored in the register specified. During this time, "REG N" will be displayed on the front panel (where N is the register number entered).

When the counter finishes setting the counter up, a reset will be generated.

ONE-SHOT/RESET SPC INDICATOR:OFF SPECIAL SB:OFF

SPECIAL FUNCTION 74 --- Relative Frequency Readings

When this function is activated, the counter assigns a negative value to the last input frequency reading and enters it into the frequency offset register (overwriting any previously entered frequency offset). The last input frequency in this case means the actual frequency of the input signal, not the frequency displayed on the front panel, which may be affected by a frequency multiplier or another special function. The counter displays the difference between the last input frequency and the current one, subject to any other functions activated. It will continue to do so until the FREQ OFFSET and CLEAR DATA keys are pressed. The OFS annunciator is turned on when this function is activated.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:ON

SPECIAL FUNCTION 75 --- Display IF Frequency Readings

When this function is activated, the counter assigns a negative value to the local oscillator (LO) frequency and enters it into the frequency offset register (overwriting any previously entered frequency offset). The counter then subtracts the LO frequency from the input frequency and displays the resulting IF frequency. It continues to do so until the FREQ OFFSET and CLEAR DATA keys are pressed. The OFS annunciator is turned on.

ONE-SHOT SPC INDICATOR:OFF SPECIAL SB:ON

SPECIAL FUNCTION 76 --- EEPROM Test

CAUTION

Care must be used when operating Special Function 76. Although the counter cannot be damaged by this function, if execution of this function is interrupted prior to completion a loss of the data contained in the EEPROM will occur. For this reason, access to this function is blocked by an internal memory protect feature. Attempting to access this function with the memory protected will cause the counter to display "ERROR 53". Refer to section 7 for information on unprotecting the memory.

This function provides the means for the user to test the EEPROM.

This function performs write and read tests on each location in the EEPROM. If any one location in the EEPROM fails the write and read tests, "ERROR 94" will be displayed. If all memory locations pass the tests, "PASSEd" will be displayed.

This function requires approximately eight minutes to complete. During those eight minutes, the counter will not respond to any entry from the keyboard.

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 90 --- Display and/or Alter GPIB Address

When this function is activated, the counter displays the current address of the GPIB interface. If the address need not be changed, the function may be terminated by pressing the CLEAR DISPLAY or CLEAR DATA keys.

After this function has been activated, the GPIB address can be changed by entering a two-digit number between 01 and 99. The function is terminated and the display returned to displaying measurement results after the second digit key is released.

(Refer to the GPIB interface section, page 4-16, for meanings of GPIB addresses above 31.)

ONE-SHOT SPC INDICATOR:ON SPECIAL SB:ON

SPECIAL FUNCTION 91 --- YIG DAC Automatic Calibration

CAUTION

Care must be used when operating Special Function 91. Although the counter cannot be damaged by this function, improper operation of it can affect the counter calibration. For this reason, access to this function is blocked by an internal memory protect feature. Attempting to access this function with the memory protected will cause the counter to display "ERROR 53".

This function is used to calibrate the Band 2 input filter. Refer to the service manual for more information on the memory protect feature and operation of this function.

SPECIAL FUNCTION 92 --- Gate Accuracy Calibration

CAUTION

Care must be used when operating Special Function 92. Although the counter cannot be damaged by this function, improper operation of it can affect the counter calibration. For this reason, access to this function is blocked by an internal memory protect feature. Attempting to access this function with the memory protected will cause the counter to display "ERROR 53".

This function is used for calibration of the counter. Refer to the service manual for more information on the memory protect feature and operation of this function.

ERROR MESSAGES

When an error occurs, an error number will be displayed. The probable cause of each error is listed below.

01 KEY PUSHED NOT FUNCTION KEY
02 LOWER LIMIT HIGHER THAN HIGH LIMIT
03 LIMITS ENTRY ONLY IN BAND 2
04 CENTER FREQUENCY ENTRY ONLY IN BAND 2 OR BAND 3
05 CENTER FREQUENCY ENTRY OUTSIDE CURRENT BAND RANGE
06 NO VALID DATA IN STORAGE REGISTERS FOR RECALL FEATURE
07 CONVERTER UNABLE TO LOCK ON SIGNAL DURING SPECIAL
09 ILLEGAL REGISTER ENTRY
10 ILLEGAL BAND ENTRY
11 ILLEGAL SUBBAND ENTRY
12 ILLEGAL RESOLUTION ENTRY
13 ILLEGAL SPECIAL FUNCTION ENTRY
14 ILLEGAL AVERAGE ENTRY
15 ILLEGAL MULTIPLIER ENTRY
16 ILLEGAL FREQUENCY OFFSET ENTRY
17 ILLEGAL CENTER FREQUENCY ENTRY
18 ILLEGAL MINPRF ENTRY
19 ILLEGAL LOW LIMIT ENTRY
20 ILLEGAL HIGH LIMIT ENTRY
21 ILLEGAL SAMPLE RATE ENTRY
22 ILLEGAL SRQ NUMBER ENTRY
23 ILLEGAL GPIB ADDRESS
24 ILLEGAL VCO FREQUENCY 1 ENTRY
25 ILLEGAL VCO FREQUENCY 2 ENTRY
26 ILLEGAL YIG FREQUENCY 1 ENTRY
27 ILLEGAL YIG FREQUENCY 2 ENTRY
28 ILLEGAL YIG DAC FREQUENCY ENTRY
29 FREQUENCY OVERFLOW DUE TO MULTIPLIER
30 PULSE PARAMETERS MEASUREMENTS GREATER THAN SPECIFIED MINPRF
31 GPIB INPUT MESSAGE TOO LONG
32 GPIB MESSAGE STARTS WITH A NUMBER
33 GPIB MESSAGE STARTS WITH A WRONG NUMBER
34 UNIDENTIFIED WORD FOUND
35 WORD MISSPELLED
36 MISSING SPACE
37 WRONG MODE ARGUMENT
40 NON-NUMERIC PARAMETER VALUE
41 WRONG FREQUENCY TERMINATOR
42 WRONG TIME TERMINATOR
43 WRONG OUTPUT ARGUMENT

44 NUMERIC ARGUMENT SYNTAX ERROR
45 NUMERIC MANTISSA HAS TOO MANY DIGITS
46 NUMERIC EXPONENT HAS TOO MANY DIGITS
47 HEX DATA SHOULD PRECEDE WITH A ZERO
48 NO HEX MEMORY ADDRESS SPECIFIED
49 ILLEGAL HEX DATA ENTRY
50 ILLEGAL HEX ADDRESS ENTRY
51 ACTIVATE SPC 72 AND 73 through STORE AND FETCH
52 ILLEGAL ENTRY
53 ACCESS TO THIS FUNCTION BLOCKED BY MEMORY PROTECT SWITCH
60 RAM FAULT
61 ROM CHECK SUM ERROR: ADDR 4000 TO 7FFF
62 ROM CHECK SUM ERROR: ADDR 8000 TO BFFF
63 ACTIVATE SPC 72 AND 73 THRU STORE AND FETCH
71 COUNT CHAIN BOARD MISSING
72 GATE GENERATOR BOARD MISSING
90 NO KEY RELEASE DETECTED
91 OPTION NOT INSTALLED
92 BAND 3 OPTION IN A 585B UNIT
93 BAND 3 WITH NO BAND 1 BOARD
94 NONVOLATILE MEMORY FAILURE
99 NO IF DETECTED

SECTION 4
PROGRAMMING

REMOTE PROGRAMMING

GENERAL PURPOSE INTERFACE BUS

The GPIB interface of the 585B/588B counters conforms to the IEEE Code and Format conventions and the IEEE 488-1978 Standards. With the GPIB interface, the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 bus interface. At the simplest level, the counter can output data to other devices, such as a thermal printer. In more sophisticated systems, an instrument controller or computer can program the counter remotely, trigger measurements, and read results. A quick reference list of GPIB commands is located in Appendix A at the end of this manual.

GPIB FUNCTIONS IMPLEMENTED

The following GPIB interface function subsets are implemented:

Interface Function	Subset	Description
SOURCE HANDSHAKE	SH1	Complete capability
ACCEPTOR HANDSHAKE	AH1	Complete capability
TALKER	T5	Basic talker, serial poll, talk only mode, unaddress if MLA
LISTENER	L4	Basic listener, unaddress if MTA
SERVICE REQUEST	SR1	Complete capability
REMOTE/LOCAL	RL1	Complete capability
DEVICE CLEAR	DC1	Complete capability
DEVICE TRIGGER	DT1	Complete capability

The 585B/588B counters thus have the capacity to provide the following capabilities in remote operation to the user:

- Acceptance of device-dependent messages to set the instrument measurement mode and parameters. The input buffer can store up to 256 characters accepted from the bus. Execution of the device-dependant messages starts after the first message separator is accepted. Input of more characters will interrupt the execution so that the additional characters are accepted and stored for fast bus response (unless buffer is full).
- Output of measurement results or any parameter value or instrument mode on demand from the system controller.
- Configuration of the output format in several ways to accommodate different system controllers and speed requirements.
- Implementation of device clear and selected device clear function to configure the instrument to the power-on state. See page 4-14 for the counter's power-on configuration.
- Implementation of group execute trigger (GET) message to start a new measurement cycle.
- Implementation of serial poll functions to allow the system controller to get a status byte from the instrument that gives status information for various functions. The instrument can also be instructed to interrupt (SRQ) the controller on any ORed combination of the status events.

- Implementation of remote/local transitions. When the counter is in remote, all front and rear panel keys and switches are disabled (except the POWER switch). Remote/local transitions will not change any instrument configuration (except the sample rate settings, which will override in a remote-to-local transition). When the counter changes from local to remote functioning, or vice-versa, all stored information is retained. The counter will operate in the same state as it was in before the change. The only exception is when the counter is performing a special function, the special function will be terminated.
- Implementation of local lockout, with the INIT/LOCAL key disabled accordingly. When the counter is in remote, and local lockout is not active, the INIT/LOCAL key on the front panel acts as the return-to-local key.
- Availability of counter configuration information, in addition to the status events available in the status byte, by means of a special OUTPUT CONFIGURATION command. When the counter is configured as a talker, it will output five bytes that contain the current configuration.
- Recognition of all three bus terminators: CR LF (carriage return line feed), NL (null), and EOI (end or identify).
- Availability of front panel annunciators for remote (RMT), talker (TLK), listener (LSN), and (SRQ) that continuously show the interface state.
- Implementation of talk-only modes for no-controller applications.

DEVICE-DEPENDENT MESSAGES (LISTENER FEATURES)

A device-dependent message generally consists of reserved words and numbers. The message structure depends on the type of message, and can be:

- Header only
- Header and argument
- Header and argument and terminator

Where the header is a reserved word, the argument is a number or a reserved word, and the terminator is a reserved word.

Messages can be concatenated with a comma (,) or semicolon (;) as separators. A message chain can be terminated with CR LF or NL or EOI. Any device-reserved word will be recognized by at least two first characters, with the exception of RESET which requires the first four letters to be entered. These first two characters are printed in **large boldface** type in the following command lists and in program examples to promote user familiarity with the shortened form of the command. Spelling of more characters (up to the full word) is optional for user program readability.

Example: INITIALIZE
INITIAL
INIT
IN
are all recognized equivalently.

A <number> can be sent in any of the defined IEEE formats (NR1, NR2, NR3).

Example: 12000
12000.00
001.2e4
.12000E+5
are all recognized equivalently.

The reserved word DEFAULT can replace a numeric argument for default value assignment.

The terminator in the parameter messages group is optional, and defaults to Hz or seconds.

A command message having more than one word (e.g., PERIOD ON) should have a space between words. However, this is optional if the second word is a number (OFFSET4.3e9 and OFFSET 4.3E9 are recognized equivalently). Additional spaces in front of words, between words, or after a message are optional, and will be ignored. Nulls and CRs are ignored anywhere. Both upper case and lower case characters are equally acceptable.

Following are the possible GPIB command messages for the 585B/588B series of counters.

Control Messages

Control, mode, and parameters messages are all used with the controller in the listener mode to enter instructions and data.

Header	Argument	Terminator	Description
CLEARDISPLAY	None	None	Returns the display to normal measurement results display, clear error. (Equivalent to front panel CLEAR DISPLAY key.)
INITIALIZE	"	"	Reconfigures the instrument to power-on state. (Equivalent to front panel INIT/LOCAL key.)
RESET	"	"	Resets counter to restart a new signal measurement cycle. (Equivalent to front panel RESET key.)
TRIGGER	"	"	Triggers a new measurement cycle. (Equivalent to front panel TRIG key.)

Mode Messages

Header	Argument	Terminator	Description
DYNAMIC	ON or OFF	None	Suppresses blanks when counter is configured in talker mode for faster free-field data transfer.
EXTERNAL	"	"	Selects the INT/EXT time base reference. (Special Function 08 can also be used to select the external time base.)
HEADER	"	"	Adds an alpha header and terminator for talker.
HOLD	"	"	Holds the last result if on. (Equivalent to front panel HOLD.)
PERIOD	"	"	Turns pulse period measurement on or off or DEFAULT. (Equivalent to front panel PULSE PERIOD key.)
SCIENTIFIC	"	"	Selects scientific notation for talker.
SEPARATE	"	"	Replaces the commas with CR LF between multinumber results.
WIDTH	"	"	Turns pulse width measurement on or off. (Equivalent to front panel PULSE WIDTH key.)

NOTE

In the local mode, SAMPLE RATE and HOLD are controlled via the front panel control, but in remote the front panel control has no effect. In the remote mode, both SAMPLE RATE and HOLD are under software control. Refer to GPIB SAMPLE RATE and HOLD commands.

Parameter Messages

Header	Argument	Terminator	Description
AVERAGE	<number>	None	Inputs an averaging value (01 to 99).
BAND	"	"	Selects a specific band (0 to 3) or DEFAULT.
CENTERFREQ	"	(Hz/kHz/MHz/GHz)	Sets a center frequency value and mode.
FETCH	"	None	Recalls counter setup stored in specified storage register (0 to 9). (Special Function 73.)
HIGHLIMIT	"	(Hz/kHz/MHz/GHz)	Sets a frequency limit high value.
LOWLIMIT	"	"	Sets a frequency limit low value.
MEMORY	<hex_adrs>	<hex_data>	Accesses a memory location and alters it (altering is optional). (Special Function 46.)
MEMORY	INCREMENT	"	Accesses the next memory location. (Special Function 46.)
MEMORY	DECREMENT	"	Accesses the previous memory location. (Special Function 46.)
MINPRF	<number>	(Hz/kHz/MHz/GHz)	Sets a minimum PRF value.
MULTIPLIER	"	None	Inputs a multiplier value (01 to 99).
OFFSETFREQ	"	(Hz/kHz/MHz/GHz)	Sets a frequency offset value.
RESOLUTION	"	None	Sets the frequency measurement resolution (0 to 9).
SAMPLERATE	"	(s/ms)	Sets a delay between measurement values (0 to 100 sec, 10 ms resolution).
SPECIAL	"	None	Activates a specific special function (00 to 99).
SRQMASK	"	"	Selects the ORed combination of status events to cause a service request.
STORE	"	"	Stores current counter setup in specified storage register (0 to 9). (See Special Function 72.)
SUBBAND	"	"	Selects a specific Band 3 subband (1 to 6)
V1FREQ	"	(Hz/kHz/MHz/GHz)	Sets a start frequency for VCO sweep (Special Functions 41, 42).
V2FREQ	"	"	Sets a stop frequency for VCO sweep (Special Functions 41, 42).
Y1FREQ	"	"	Sets a start frequency for YIG sweep (Special Function 40).
Y2FREQ	"	"	Sets a stop frequency for YIG sweep (Special Function 40).

Output Control Messages

These commands are used with the controller in the talker mode to request the output of data.

Command	Description
OUTPUT AVERAGE	Outputs the last specified averaging value.
OUTPUT BAND	Outputs the number of the last specified band.
OUTPUT CENTERFREQ	Outputs the center frequency last specified.
OUTPUT CONFIGURATION	Outputs current configuration of instrument. See page 4-13.
OUTPUT DATE	Outputs a 42-character string that shows the revision level and date.
OUTPUT DEFAULT	Outputs displayed data.
OUTPUT ERRORNUMBER	Outputs the number of the last error. See listing of error numbers on page 3-35.
OUTPUT FREQUENCY (AND WIDTH) (AND PERIOD)	Controls which measurement results to output. (Note: More than one measurement result is optional. The order of the results is preserved in the output. Output frequency, width and period can be used in any combination.)
OUTPUT HIGHLIMIT	Outputs the high frequency limit last specified.
OUTPUT IDENTIFICATION	Outputs "EIP58nB GPIB dd", where n is 5 or 8 and dd is the GPIB address.
OUTPUT KEYCODE	Outputs the code of the last key pressed.
OUTPUT LEVEL	Outputs the rough amplitude measurement result (Special Function 20).
OUTPUT LOWLIMIT	Outputs the low frequency limit last specified.
OUTPUT MEMORY	Outputs the content of the memory in the last accessed location (Special Function 46).
OUTPUT MINPRF	Outputs the minimum PRF last specified.
OUTPUT MULTIPLIER	Outputs the last specified multiplier value.
OUTPUT OFFSETFREQ	Outputs the offset frequency last specified.
OUTPUT RESOLUTION	Outputs the last specified frequency measurement resolution.
OUTPUT SAMPLERATE	Outputs the last specified delay time between measurement values.
OUTPUT SETUP	Outputs a 142-character string that describes the current setup. See page 4-6.
OUTPUT SRQMASK	Outputs the combination of status events required to cause a service request. See page 4-11.
OUTPUT SUBBAND	Outputs the number of the last specified subband.
OUTPUT V1FREQ	Outputs the last specified start frequency for VCO sweep. (Special Functions 41 and 42).
OUTPUT V2FREQ	Outputs the last specified stop frequency for VCO sweep.
OUTPUT Y1FREQ	Outputs the last specified start frequency for YIG sweep (Special Function 40).
OUTPUT Y2FREQ	Outputs the last specified stop frequency for YIG sweep (Special Function 40).

Output Setup Command

The output setup command causes the counter to output a 142-character string that corresponds to the current setup of the instrument. The following sample program, for the HP-85, can be used to obtain the setup string:

```
10  DIM A$[150]                    ! Dimension a variable to hold the string
20  OUTPUT 718;"OUTPUT SETUP"      ! send command to counter
30  ENTER 718;A$                   ! get output from counter
40  DISP A$                        ! display output on HP-85
```

Setup string: BA2,SU1,RE3,AV01,MU01,OF+000000000KH,LO000900MH,HI018500MH, CE000000MH,MI0000E00,SA000040MS,SR000,SP62,SP64,SP66,SP68, SP70,SP45,PE0,WI0,HO0,EX0

The following list can be used to decode the returned setup string. The information contained in the parentheses will change depending on the current setup of the instrument.

BA2:	BAND (2)
SU1:	SUBBAND (1)
RE3:	RESOLUTION (3)
AV01:	AVERAGE (1) READING
MU01:	MULTIPLY X (1)
OF+000000000KH:	FREQUENCY OFFSET = (0)
LO000900MH:	LOW LIMIT = (900) MHz
HI018500MH:	HIGH LIMIT = (18.5) GHz
CE000000MH:	CENTER FREQUENCY = (0) NOT ACTIVE
MI0002000:	MINIMUM PRF = (2) kHz
SA000040MS:	SAMPLE RATE = (40) MILLISECONDS
SR000:	SERVICE REQUEST MASK
SP62:	SPECIAL FUNCTION (62) ACTIVE
SP64:	SPECIAL FUNCTION (64) ACTIVE
SP66:	SPECIAL FUNCTION (66) ACTIVE
SP68:	SPECIAL FUNCTION (68) ACTIVE
SP70:	SPECIAL FUNCTION (70) ACTIVE
SP45:	SPECIAL FUNCTION (45) ACTIVE
PE0:	PULSE PERIOD = (0) OFF
WI0:	PULSE WIDTH = (0) OFF
HO0:	HOLD = (0) OFF
EX0:	TIME BASE = (0) INTERNAL

Syntax Definition

In the instructions that follow, | means "or" and N|S means "null or space." The format used for the examples is that used for the HP 85 controller. Sample formats for other controllers are also shown.

DEVICE-DEPENDENT MESSAGE:	<message><N|S><message terminator>|<message> <message separator><message><message terminator>
Message	<control message>|<mode message>|<parameter message>|<output control message>
Message separator	,|;
Message terminator	CR LF|NL|EOI

1. CONTROL MESSAGE: INITIALIZE|RESET|TRIGGER|CLEAR DISPLAY

   Example: To instruct the instrument to begin a new signal acquisition process, the operator enters: OUTPUT 718;"RESET"

2. MODE MESSAGE: <mode name><space><mode position>

   Mode name: WIDTH|PERIOD|HOLD|EXTERNAL|SCIENTIFIC|SEPARATE|HEADER|DYNAMIC

   Mode position: ON|OFF|1|0|DEFAULT

   Example: To instruct the instrument to an external reference, the operator enters: OUTPUT 718;"EXTERNAL ON"

3. PARAMETER MESSAGE: <parameter message 1>|<parameter message 2>|<parameter message 3>|<parameter message 4>|<parameter message 5>

   - PARAMETERS MESSAGE 1: <parameter 1><N|S><argument>

     Parameter 1: BAND|SUBBAND|RESOLUTION|SPECIAL|AVERAGE|MULTIPLIER|SQRMASK|GPIBADDRESS

     Argument: DEFAULT|<number>

     Number: <NULL|+|><mantissa><exponent>

     Mantissa: <digit>|<digitstring>|<digit|digit string,digit|digit string>

     Exponent: NULL|E<NULL|+|><digit|digit string>

     Example: To instruct the instrument to accept an averaging value, the operator enters: OUTPUT 718;"AVERAGE 70"

   - PARAMETER MESSAGE 2: <parameter 2><N|S><argument>N|S<frequency terminator>

     Parameter 2: OFFSETFREQ|HIGHLIMIT|LOWLIMIT|MINPRF|CENTER FREQ|Y1FREQ|Y2FREQ|Y3FREQ|V1FREQ|V2FREQ

     Frequency terminator: NULL|Hz|kHz|MHz|GHz

     Example: To instruct the instrument to accept a frequency high limit value, the operator enters: OUTPUT 718;"HIGHLIMIT 12.3 GHz" or "HIGHLIMIT 12.3E6 kHz"

   - PARAMETER MESSAGE 3: SAMPLERATE<N|S><argument><N|S><time terminator>

     Time terminator: NULL|SEC|MSEC

     Example: To instruct the instrument to accept a sample rate value, the operator enters: OUTPUT 718;"SAMPLERATE 100 MSEC"

- PARAMETER MESSAGE 4: MEMORY<N|S><memory instruction><N|S><memory data>

  Memory instruction — INCREMENT|DECREMENT|<memory location>

  Memory location — 0<hex digit><hex digit><hex digit><hex digit>

  Hex digit — <digit>|A|B|C|D|E|F

  Memory data — NULL|0<hex digit><hex digit>

  Example: To instruct the instrument to change memory location 99AF to 3B, the operator enters: OUTPUT 718;"MEMORY O99AF 03B"

- PARAMETER MESSAGE 5: STORE|FETCH<N|S><NUMBER>

  Example: To instruct the instrument to store or recall a counter setup in a specified storage register, the operator enters: OUTPUT 718; "STORE 03" or OUTPUT 718;"FETCH 03."

4. OUTPUT CONTROL MESSAGE: OUTPUT<SPACE><output parameter>

   Output parameter — <single parameter>|<result parameter>

   Single parameter — RESOLUTION|BAND|SUBBAND|AVERAGE|MULTIPLIER|ERRORNUMBER|SQRMASK|CONFIGURATION|LEVEL|MEMORY|IDENTIFICATION|LOWLIMIT|HIGHLIMIT|OFFSETFREQ|CENTERFREQ|MINPRF|SAMPLERATE|KEYCODE|SETUP

   Result parameter — DEFAULT|<result list>

   Result list — <result name>|<result name>SPACE>AND<SPACE><result name>|<result name>SPACE>AND-SPACE><result name>SPACE>AND<SPACE><result name>

   Result name — FREQUENCY|WIDTH|PERIOD

   Example: To request the controller to display the width and frequency, in that order, the operator enters:

```
OUTPUT 718;"OUTPUT WIDTH AND FREQUENCY"
ENTER 718; A$
DISP A$
```

Output and Format Examples

The following programs illustrate how controllers function with the counter and how different kinds of controllers give instructions. These programs set the counter up in a sample configuration and program it to make a series of measurements of a 12.5 GHz pulsed signal with 13.258 μs period. The talk and listen address of the counter is assumed to be 18.

- Hewlett Packard 85

```
10 DIM A$[36]
20 OUTPUT 718;"IN"
30 WAIT 4000
40 OUTPUT 718;"PE ON,RE 4"
50 OUTPUT 718;"HI 17.5 GHZ,LO 1.1 GHZ"
60 WAIT 1000
70 OUTPUT 718;"OUTPUT WI AND FR"
80 WAIT 1000
90 ENTER 718;A$
100 DISP A$
110 END
```

This program initializes the counter, provides a resolution value and a high and low frequency limit, and instructs it to output pulse width to the counter display and pulse width and frequency to the controller display. The controller display would appear something like this:

0.0000132580 12500000000

- Hewlett Packard 9825A

```
0: dim A(10)
1: rem 7
2: wrt 718,"BA 2,RE 4,OF - 4.55 MHZ"
3: wait 300
4: For I = 1 to 10
5: red 718, A(1)
6: prt A(1)
7: next I
8: end
```

The HP 9825A program will cause the counter to take a series of ten readings, print them on the HP 9825A paper tape, and stop. Notice that an offset of 4.55 MHz is subtracted from each reading.

- Hewlett Packard 9845A

```
10: OUTPUT 718,"BA 3, RE 4, OF -4.55 MHZ"
15: WAIT 300
20: INPUT 718,A
30: PRINT "Frequency minus offset equals,"A
40: GO TO 20
```

- Tektronix 4051

```
10: PRINT @ 18:"BA 3,RE 4, OF -4.55 MHZ"
20: INPUT @ 18:A
30: PRINT "Frequency minus offset equals,"A
40: GO TO 20
```

The programs shown for the HP 9845A and Tektronix 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a STOP command. This is accomplished on the HP 9845A with the key labeled STOP and on the Tektronix 4051 with the key labeled BREAK. To restart the program, enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

OUTPUT MESSAGES (TALKER FEATURES)

After receiving a talk address, the GPIB will output the current configuration, or any parameter value or measurement result, in response to the appropriate output control message. After power-on or device-clear, the controller outputs the displayed measurement results (as it does after the OUTPUT DEFAULT command).

The controller can be instructed to output any ordered combination of the three possible measurements, no matter what is displayed on the front panel.

Examples: OUTPUT FREQ AND WIDTH
OUTPUT WIDTH AND PERIOD
OUTPUT WIDTH AND FREQUENCY AND PERIOD

The format of each output message can be controlled using the following:

- SCIENTIFIC – provides exponential notation with engineering exponents when SCIENTIFIC is ON. Default is OFF.
- DYNAMIC – suppresses blanks and trailing zeros for faster data transfers when DYNAMIC is ON. Default is OFF.
- HEADER – provides an alpha header and terminator around each numeric data item for clarity, (useful for printers) when HEADER is ON. Default is OFF.

NOTE

Terminator takes over the exponential role if both SCIENTIFIC and HEADER are ON.

- SEPARATE – Substitutes CR LF for the comma between results of one measurement (freq,period) when SEPARATE is ON. Default is OFF.
- DEFAULT – Outputs data in default format. The fixed fields are 16 characters long for the header and argument, and 5 long for the terminator. When none of the output formatting features above are turned on, numbers are right justified, letters are left justified, blanks are filled.

Example: The counter is measuring a 12.34 GHz pulsed signal with 98 ns width and 14.567 µs period. The operator enters the following messages through the controller:

RESOLUTION 6
OUTPUT FREQ AND WIDTH AND PERIOD

The output for each message format will be as follows (b is for blank):

Parameter	Output
Default:	bbbbb12340000000,bbbbb0.000000100,bbbbb0.000014570 CR LF
SCIENTIFIC on:	bbbbbbbb12.340E+9,bbbbbbbbbb100E-9, bbbbbbbb14.57E-6 CR LF
DYNAMIC on:	34E9,100E-9,14.57E-6 CR LF
SEPARATE on:	2.34E9 CR LF 100E-9 CR LF 14.57E-6 CR LF
HEADER on:	FREQUENCY 12.34 GHz CR LF WIDTH 100 NSEC CR LF PERIOD 14.57 USEC CR LF

If the counter is searching, zero data will be output to the controller on all results once every search loop. If the counter has found a signal, a measurement result will be output only once.

When the instrument is in HOLD, therefore, the user must trigger the counter before sending another talk address. Otherwise, since it has no data to output, the counter will hold indefinitely.

STATUS BYTE

Both the 585B and 588B counters maintain a one byte register that contains current information on the status of the instrument. This register, called the status byte, can be accessed through the GPIB using the serial poll command. When serial polled, the counter responds by returning a numeric value between 0 and 256. This value is the weighted sum of the status bits which are set. The status byte is structured as follows:

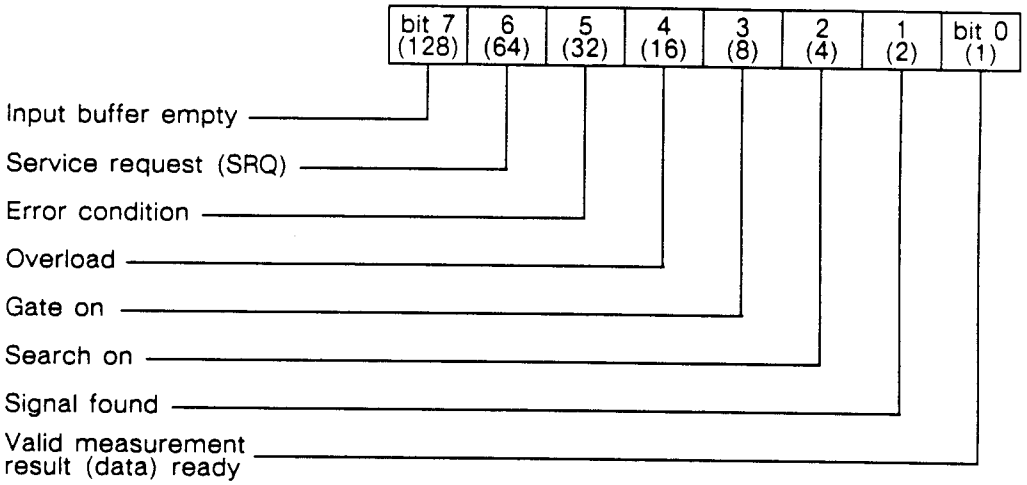

Figure 4-1. Status Byte Structure.

For example, execute the following commands using an HP 85.

```
10 A=SPOLL(718)
20 DISP A
30 END
```

With no signal applied to the counter, the value displayed on the HP 85 controller should be 132. Since the value is the weighted sum of all the bits set in the status byte, a value of 132 indicates that the GPIB input buffer is empty and the counter is in the search mode.

SERVICE REQUEST MASK

The counter can be instructed to send an interrupt, by setting the SRQ line on the GPIB, when any ORed combination of the bits in the status byte are set. This is done by sending the counter a service request mask.

For example, to instruct the counter to generate an SRQ whenever it has valid data available or an error condition exists, send the following service request mask:

```
OUTPUT 718;"SRQMASK 33"
```

This would tell the counter to generate an SRQ whenever bit 0 and bit 5 of the status byte are set. Since bit 0 corresponds to valid measurement result ready and bit 5 corresponds to an error condition, the counter would generate an SRQ whenever either an error condition exists or a valid measurement is available.

The following items should be included in any program using the SRQ feature:

1. Tell the counter when to generate an SRQ. That is, tell the counter which events should generate an SRQ. This is done using the SRQMASK command.

2. Tell the controller to monitor the SRQ line on the GPIB. The SRQ is a maskable interrupt and the controller needs to know if it should respond to the interrupt.

3. Tell the controller what to do when it receives an SRQ interrupt.

4. Serial poll the counter after an SRQ is generated to clear the interrupt. When the counter generates an SRQ it sets bit 6 in the status byte. Serial polling the instrument clears the SRQ bit and allows the instrument to generate a new SRQ upon the next occurrence of the conditions specified in the SRQ Mask.

5. It may also be necessary to clear the SRQ register in the controller. Consult your manual on the controller for more information on clearing the SRQ register in the controller.

The following program, written on an HP 9826, demonstrates how to use the SRQ feature to obtain a valid measurement from the counter.

```
10  ASSIGN @COUNTER TO 718          ! Assigns 718 to address variable
                                    ! The number 7 is the GPIB interface
                                    ! and 18 is the counter's GPIB address
20  REMOTE @COUNTER                 ! Place counter in remote
30  OUTPUT @COUNTER;"SRQMASK 1"     ! Send SRQ mask to counter
40  ENABLE INTR 7;2                 ! Enable interrupt in controller
50  ON INTR 7 GOTO FLAG             ! Tell controller how to handle interrupt
70  WAITING:                        ! Label
60  PRINT "WAITING FOR VALID MEASUREMENT"
80  GOTO WAITING
90  FLAG: PRINT "***** SRQ RECEIVED *****"
100 ENTER @COUNTER;FREQ             ! Input frequency from counter
110 PRINT "FREQ = ";FREQ            ! Print frequency
120 S2 = SPOLL(@COUNTER)            ! Clear SRQ bit in counter
130 STATUS 7,4;S                    ! Clear SRQ bit in controller
140 OUTPUT @COUNTER;"SRQMASK 00"    ! Turn off SRQ mask in counter
150 OFF INTR 7                      ! Turn off interrupt in controller
160 END                             ! Program end
```

To demonstrate this program, set up counter with no signal applied and start the program running. The controller should continually print out "WAITING FOR VALID MEASUREMENT". Then apply a signal. As soon as the counter finds the signal and counts it, the controller will print out the frequency of the signal.

CONFIGURATION INFORMATION

Counter configuration information is accessible via five configuration bytes. After receiving the OUTPUT CONFIGURATION message and then being addressed to talk, the controller will output five ASCII characters, the symbols for the decimal equivalents of the setting of the status bytes. The bytes are structured as follows:

	bit 7	6	5	4	3	2	1	bit 0
Byte 1 Options and Measurement Mode	PERIOD on/ off	WIDTH on/ off	UDF	UDF	UDF	BAND3 Opt.	BAND1	585B or 588B

	bit 7	6	5	4	3	2	1	bit 0
Byte 2 Parameters Condition	UDF	UDF	AVG	FREQ MULT	FREQ OFST	CENTER FREQ	HIGH LIMIT	LOW LIMIT

	bit 7	6	5	4	3	2	1	bit 0
Byte 3 Specials State	UDF	PP ONLY on/ off	PRF on/ off	STOP on/ off	SAMPL on/ off	TRACK on/ off	DISP on/ off	SPECIAL on/ off

	bit 7	6	5	4	3	2	1	bit 0
Byte 4 Interface and Switch State	UDF	UDF	UDF	UDF	EXT	HOLD	SRQ	REMOTE

	bit 7	6	5	4	3	2	1	bit 0
Byte 5 Format Configuration	UDF	UDF	UDF	UDF	DYNAM on/ off	SEPAR on/ off	HEADR on/ off	SCIEN on/ off

The program below is an example of how to query the status bytes for configuration information. The counter model number is determined by checking byte 1, bit 0.

```
10 OUTPUT 718; "OUTPUT CONFIGURATION"
20 ENTER 718; A$
30 PRINT "CONFIGURATION STRING = ";A$
40 B$=A$[1,1]
50 PRINT "FIRST BYTE = ";B$
60 Y=NUM(A$)
```

```
70 IF BIT (Y,0) THEN C=588B ELSE C=585B
80 PRINT "COUNTER IS EIP"; C
90 END
```

The controller would output:

```
CONFIGURATION STRING = +%X-[
FIRST BYTE = *@+//
COUNTER IS EIP 588B
```

DEFAULT STATE (DEVICE CLEAR FEATURES)

The default state of the instrument occurs after power-on, hardware initialization, or a device clear command. The default state can be customized using Special Function 72. For additional information on this feature, see page 3-33. The following table lists the factory-set default state values of the counter.

Parameter	Default State
Average	01
Band	2
Center frequency	0 (off)
Clear display	Activated
Converter	Reset
Display	Enabled
Dynamic	Off
External reference	Off
Frequency limit high	20.5 GHz (585B) or 26.5 GHz (588B)
Frequency limit low	900 MHz
Header	Off
Hold	Off
Minimum pulse repetition frequency	2 kHz
Multiply frequency	01
Offset frequency	00
Output	Frequency measurement data
Resolution	3 (1 kHz)
Sample rate	Maximum
Scientific	Off
Separate	Off
Special functions	Off
SRQmask	Off

GPIB ADDRESS SELECTION

This counter employs a software selectable GPIB address which is stored in nonvolatile memory. To verify the GPIB address, enter Special Function 90: the counter will display the current GPIB address. Press the CLEAR DISPLAY key to exit Special Function 90 without changing the GPIB address.

To change the GPIB address, enter Special Function 90 followed by the desired GPIB address (see Figure 4-2).

PRESS: SPECIAL FUNC [9] [0] [2] [0]

Since the GPIB address is stored in nonvolatile memory, the counter will always default to the last GPIB address selected.

ADDRESS CHARACTERS*		ADDRESS CODES					
		Binary					
Listen	Talk	5	4	3	2	1	Decimal**
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
'	L	0	1	1	0	0	12
-	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Address characters in ASCII code.

** Decimal Talk/Listen Address is provided as a cross-reference for those controllers which use decimal address.

Figure 4-2. Allowable Address Codes.

TALK ONLY MODES

The talk only modes enable the counter to continuously output data to other devices on the bus, such as a printer, without the need of an instrument controller. To use the counter in a talk only mode, enter the GPIB address corresponding to the desired data output format. The receiver must be configured to the listen only mode to enable data to transfer across the bus.

NOTE

Address is composed of the binary value of the choices +32.

Scientific	Separate	Header	Dynamic	Address
off	off	off	off	32
off	off	off	on	33
off	off	on	off	34
off	off	on	on	35
off	on	off	off	36
off	on	off	on	37
off	on	on	off	38
off	on	on	on	39
on	off	off	off	40
on	off	off	on	41
on	off	on	off	42
on	off	on	on	43
on	on	off	off	44
on	on	off	on	45
on	on	on	off	46
on	on	on	on	47

DATA INPUT AND OUTPUT SPEED

Input Speed

It takes a specific amount of time for the counter to process input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is processing input data, the data is accepted as soon as it is available on the bus and is temporarily stored in a 256-character storage memory.

It is necessary to be aware of the difference between accepting data and complying with it. If the counter is asked to output a reading before it is finished processing the input data, the output will not reflect the newly entered data. To prevent this, sufficient programmed delays must be provided (see the sample program formats on page 4-9). Bit 7 in the status byte can be used to determine if the counter has completed the processing of the GPIB command messages. Refer to the section on the status byte.

Output Speed

Several options have been provided in the GPIB interface for the user who wants to increase the output speed of the counter. Each of the following conditions increases the measurement cycle rate. The fastest measurement cycle time is achieved with all of the following conditions set:

HEADER OFF: Outputs the numeric results without header or terminator (default).

SCIENTIFIC OFF: Outputs fixed point results which are shorter than exponential notations (default).

DYNAMIC ON: Suppresses leading blanks. NOTE: The controller has to have free field capability.

SPECIAL 61: Disables the tracking feature, thus saving the time required for YIG and VCO corrections.

SPECIAL 63: Disables sample rate control, thus deleting any delay between gates. (For counter in local mode.)

SPECIAL 65: Disables the LED results display thus saving the time required for display, formatting and output.

SAMPLERATE 0: Same as SPECIAL 63 for counter in remote mode.

READING MEASUREMENTS

To read a measurement from the counter to a controller, the user must first address the counter to talk and the controller to listen. The examples below indicate how a controller may read a measurement from the counter.

- Hewlett Packard 9825A

  10 red 718,A
  20 prt A

- Hewlett Packard 9845A

  10 ENTER 718,A
  20 PRINT A

- Tektronix 4051A

  10 INPUT @ 18:A
  20 PRINT A

The EIP counter provides a choice of method for taking readings. When the command HOLD is ON, the counter takes one reading then waits for a RESET command or a device trigger GPIB command. In this condition, the counter is sent a RESET command or a device trigger and (when addressed to talk) outputs a new reading to the bus.The counter will hold that particular reading on the display until another RESET command or device trigger is received.

When the HOLD command is off, data is read out to the bus in the normal way. The display is automatically updated at the specified sample rate, and the counter outputs successive measurement readings without requiring a RESET command or device trigger each time.

SECTION 5
OPERATIONAL VERIFICATION TESTS

INTRODUCTION

This section contains information for verifying proper operation of the counter. Although these tests are not comprehensive, they do insure, to a high degree of confidence, that the instrument is operating properly. The tests can be useful for incoming inspection and should be performed after any servicing to insure proper operation of the counter. All tests can be performed without removing the instrument covers. A test report form is included at the end of this section that can be used to provide a test record. If the application is especially critical in nature, more extensive testing may be required and is covered in the performance verification test section of the service manual.

Because of the high cost and specialized nature of frequency sources above 40 GHz, testing above this frequency is not covered. Also, for the purpose of operational verification tests, simulated pulsed signals are used in Bands 1 and 3.

EQUIPMENT REQUIREMENTS

Equipment required for the operational verification tests on the EIP 585B or 588B counter is listed in Table 5-1. The critical parameters are the minimum use specifications required for the performance of the procedures, and are included to assist in the selection of alternative equipment. Satisfactory performance of alternative items should be verified prior to use. All applicable equipment must bear evidence of current calibration. For many of the following tests, an EIP 578B counter is used to source lock the microwave sweeper, thus providing a stable source for testing. This combination may be replaced by a frequency synthesizer.

Table 5-1. Equipment Requirements.

Description	Critical Parameters	Recommended Manufacturer	Model
Frequency Synthesizer	100 Hz to 10 MHz	Hewlett Packard	3325A
Sweep Generator	10 MHz to 40 GHz	Wiltron	6668B
Sweep Generator	3 GHz to 18 GHz	Wiltron	6635B
Source Locking Counter	10 MHz to 26.5 GHz	EIP	578B
Spectrum Analyzer	3 GHz to 18 GHz	Hewlett Packard	8566B
Power Meter	10 MHz to 60 GHz	Hewlett Packard	437B
Power Sensor	10 MHz to 18 GHz (-20 to +10 dBm)	Hewlett Packard	8481A
Power Sensor	950 MHz to 26.5 GHz (-20 to +10 dBm)	Hewlett Packard	8485A
Power Sensor	26.5 GHz to 40 GHz (-20 to +10 dBm)	Hewlett Packard	R8486A
Oscilloscope	100 Hz to 10 MHz	Tektronix	475
Power Splitter	10 MHz to 26.5 GHz	Hewlett Packard	11667B
Directional Coupler	950 MHz to 18 GHz	Narda	4226-10
Directional Coupler	18 GHz to 26.5 GHz	Narda	4017C-10
Pulse Generator	1 MHz	Wavetek	801
Pulse Modulator	1 GHz to 2 GHz	Hewlett Packard	8731B
Pulse Modulator	2 GHz to 18 GHz	Hewlett Packard	11720A
Pulse Modulator	18 GHz to 26.5 GHz	Narda	S214DS
3 dB Attenuator	950 MHz to 26.5 GHz	Weinschel	9-3
Cable Kit	--	EIP	590
Remote Sensor	26.5 to 40 GHz	EIP	091

SOURCE LOCKING SETUP

In some of the following tests, the EIP 578B counter is used to source lock the sweep generator to provide a stable frequency source for testing the 585B/588B counters.

The source locking setup, described below, is not limited to locking the Wiltron sweeper. It can be used to source lock almost any electronically tunable signal source over a frequency range of 10 MHz to 110 GHz. For more information on source locking the Wiltron 6600 series of sweep generators, request Application Bulletin 10 from our sales representative in your area or directly from EIP.

Regardless of the particular sweeper, the procedure for source locking is basically the same. A sample of the output from the sweeper is applied to the appropriate band on the EIP 578B counter. For the setup shown in Figure 5-1, a power splitter provides the sample. The COARSE TUNE OUT connector from the 578B counter is connected to the external sweep input on the sweeper. The ∅ LOCK OUT connector on the 578B counter is connected to the FM input on the sweeper. The FM modulation on the sweeper is enabled and the sweeper is set to the external sweep mode.

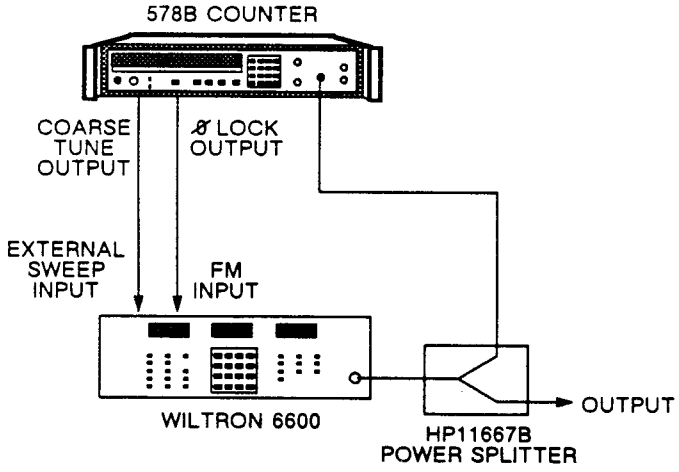

Figure 5-1. Source Locking Setup.

With the equipment set up as described above, source locking over the entire range of the sweeper can be achieved by entering the desired frequency.

For example, to lock the sweeper at 10 GHz:

PRESS: LOCK FREQ [1] [0] GHz

At this point, the sweeper should be locked to 10 GHz, the LCK annunciator on the counter should be lit, and 10 GHz should be the displayed frequency. In the following tests, the output frequency from the sweeper is controlled directly by the EIP 578B counter, while the power is controlled at the sweeper.

OPERATIONAL VERIFICATION TEST PROCEDURES

BAND 0 RANGE AND SENSITIVITY TEST (CW ONLY)

Description

This test verifies counter operation from 100 Hz to 250 MHz at -15 dBm (0.1125 V p-p into 50 ohms). The oscilloscope is used to set signal levels below 10 MHz, and the power meter is used to set signal levels at 10 MHz and above. Test setup 1 covers the frequency range from 100 Hz to 10 MHz and test setup 2 covers the range from 10 MHz to 250 MHz.

Equipment

Frequency synthesizer (Hewlett Packard 3325A)
Sweep generator (Wiltron 6668B)
Source locking counter (EIP 578B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Power splitter (Hewlett Packard 11687B)
Oscilloscope (Tektronix 475)

Test Setup 1

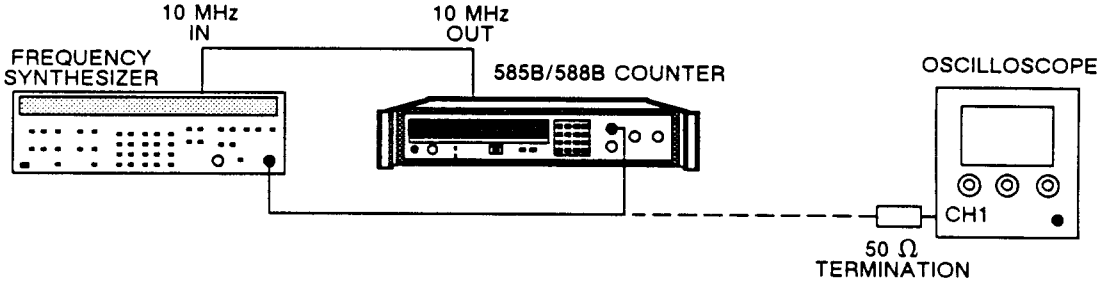

Figure 5-2. Band 0 Range and Sensitivity Test Setup (100 Hz to 10 MHz).

Procedure

1. Connect equipment as shown in Figure 5-2.
2. Set the counter to Band 0 and select resolution 2.
3. Set the output frequency from the synthesizer to 100 Hz.
4. Using the oscilloscope, set the output signal level from the synthesizer to -15 dBm (0.11 V p-p into 50 ohms).
5. Apply the 100 Hz signal to the counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 1 kHz, 10 kHz, and 100 kHz and at 1 MHz and 10 MHz.

Test Setup 2

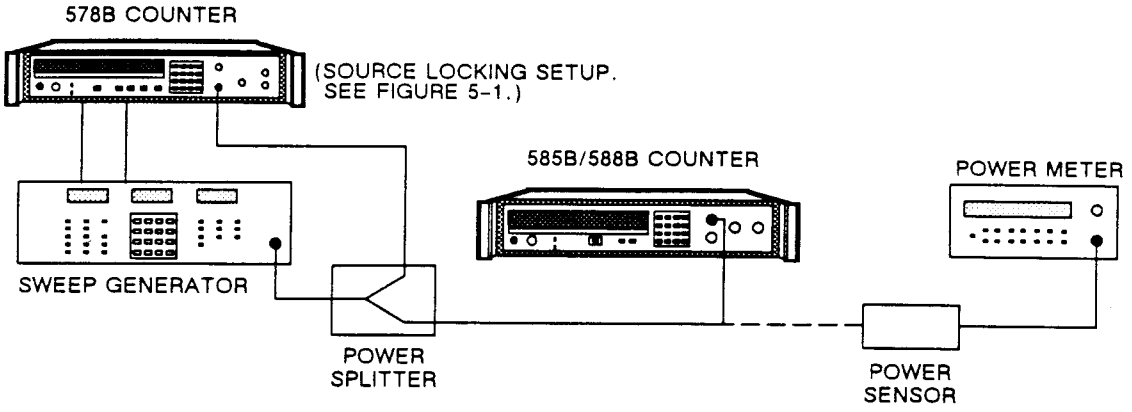

Figure 5-3. Band 0 Range and Sensitivity Test Setup (100 MHz to 250 MHz).

Procedure

1. Connect equipment as shown in Figure 5-3.
2. Set the 585B/588B counter to Band 0 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 100 MHz.
4. Using the power meter, set the output signal level from the sweeper to -15 dBm.
5. Apply the 100 MHz signal to the 585B/588B counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 200 MHz and 250 MHz.

BAND 1 RANGE AND SENSITIVITY TEST

Description

This test verifies counter operation from 250 MHz to 1 GHz at -15 dBm for both CW and simulated pulsed signals. The pulse generator is used to simulate a pulsed signal by applying a 50 ns ECL low with a 1 MHz repetition rate to the INHIBIT IN connector on the rear panel of the 585B/588B counter. The power meter is used to set signal levels.

Equipment

Sweep generator (Wiltron 6668B)
Source locking counter (EIP 578B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Pulse generator (Wavetek 801)
Power splitter (Hewlett Packard 11667B)
Oscilloscope (Tektronix 475)

Procedure

1. Connect equipment as shown in Figure 5-4.
2. Set the 585B/588B counter to Band 1 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 250 MHz.
4. Using the power meter, set the output signal level from the sweeper to -15 dBm.

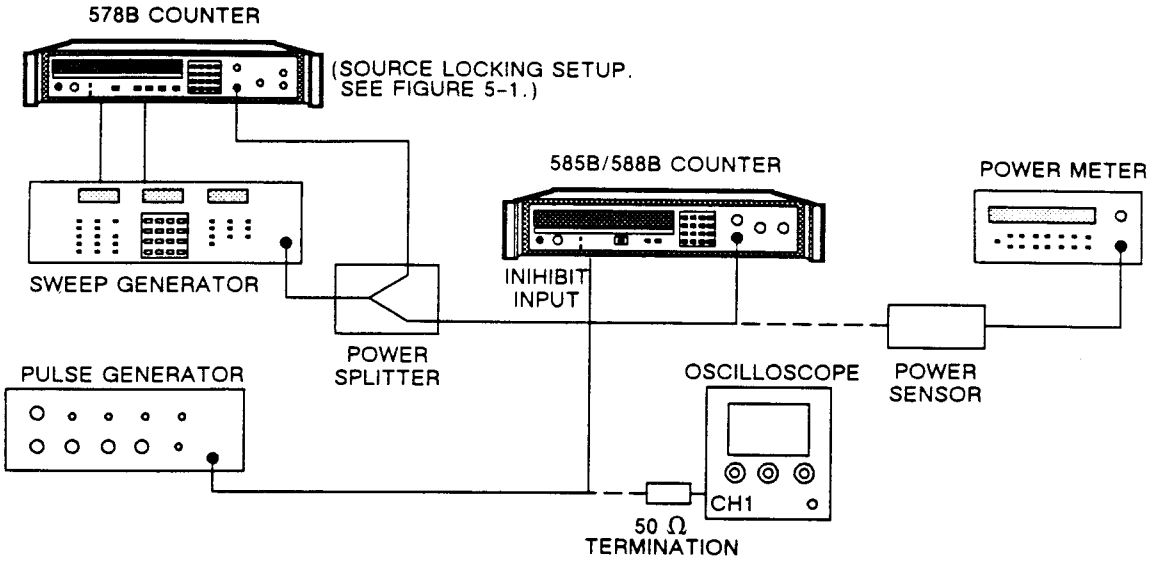

Figure 5-4. Band 1 Range and Sensitivity Test Setup.

5. Apply the 250 MHz signal to the counter, verify proper reading, and record the results.

6. Repeat steps 3, 4, and 5 at 300 MHz, 400 MHz, 500 MHz, 600 MHz, 700 MHz, 800 MHz, 900 MHz and 1 GHz.

7. Using the oscilloscope, set up the pulse generator to output a 50 ns wide ECL low signal with a 1 MHz pulse repetition rate. Apply the signal to the INHIBIT IN connector on the rear panel of the 585B/588B counter. This signal gates signal threshold inside the counter and is used to simulate a pulsed signal.

8. Repeat steps 3, 4, 5, and 6 for the simulated pulsed signal and record the results.

BAND 2 RANGE AND SENSITIVITY TEST

Description

This test verifies counter operation from 950 MHz to 20 GHz (26.5 GHz for the 588B counter). The first part of the test verifies operation in the CW mode. Next, the counter is tested in the pulse mode using the pulse modulators to modulate the microwave source. Attenuators are necessary on the input and output of the pulse modulators to reduce frequency pulling of the microwave source. To be able to accurately set the power level of the pulsed signal, it is necessary to compensate for the insertion loss of the pulse modulators by applying a constant enable signal to the pulse modulator and adjusting the sweeper at each test frequency until the output power from the modulator is at the required level.

Equipment

Sweep generator (Wiltron 6668B)
Source locking counter (EIP 578B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8485A)
Pulse generator (Wavetek 801)
Pulse modulator (Hewlett Packard 8731B)
Pulse modulator (Hewlett Packard 11720A)
Pulse modulator (Narda S214DS)

Power splitter (Hewlett Packard 11667B)
Directional coupler (Narda 4226-10)
Directional coupler (Narda 4017C-10)
3 dB attenuator (2) (Weinschel 9-3)

Test Setup 1

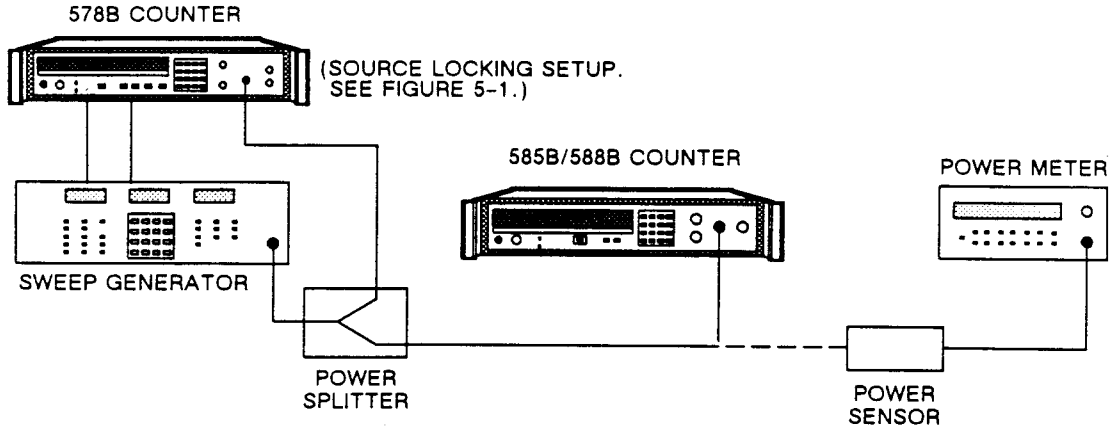

Figure 5-5. Band 2 CW Signal Range and Sensitivity Test Setup.

Procedure

1. Connect equipment as shown in Figure 5-5.
2. Set the counter to Band 2 and select resolution 3.
3. Using the EIP 578B counter, source lock the sweeper at 950 MHz.
4. Using the power meter, set the output signal level from the sweeper to -20 dBm.
5. Apply the 950 MHz signal to the 585B/588B counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 1 GHz, 3 GHz, 6 GHz, 10 GHz, 12.4 GHz, 15 GHz, 18 GHz, and 20 GHz. For Model 588B counters, also test at 22 GHz, 24 GHz, and 26.5 GHz.

Test Setup 2

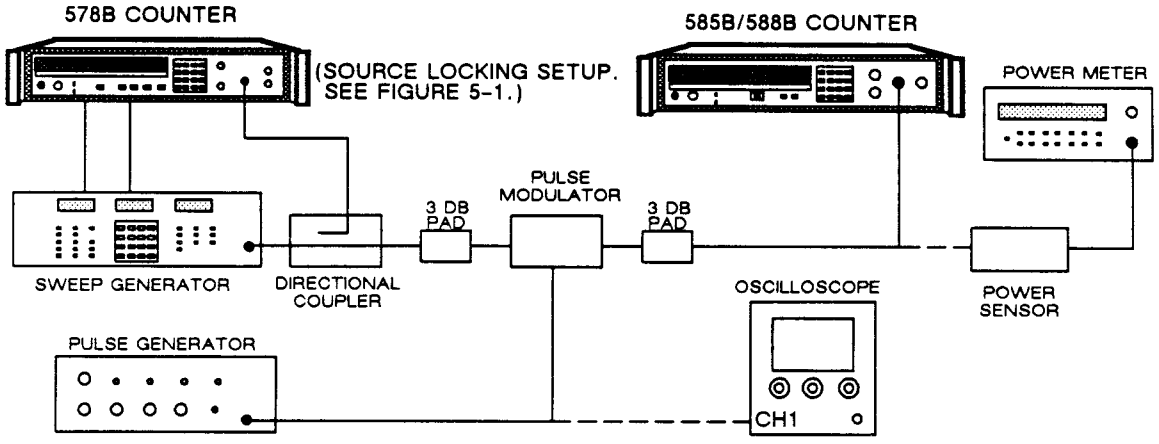

Figure 5-6. Band 2 Pulsed Signal Range and Sensitivity Test Setup

Procedure

For this test, three pulse modulators and two directional couplers are used. Use the devices that correspond to the frequency under test. See Table 5-1 for a listing of frequency ranges of the pulse modulators and directional couplers.

1. Connect equipment as shown in Figure 5-6.
2. Set the counter to Band 2 and select resolution 3.
3. Using the oscilloscope, set the pulse generator to output a 100 ns wide TTL signal with a 1 MHz repetition rate. This signal will be used to drive the pulse modulators.
4. Using the EIP 578B counter, source lock the sweeper at 950 MHz.
5. Apply a constant enable signal from the pulse generator to the pulse modulator. Adjust the output power on the sweep generator until the power meter indicates the specified sensitivity level for the counter.
6. Apply the modulation drive from the sweep generator to the appropriate pulse modulator and connect the pulse modulated signal to the counter.
7. Verify that the counter counts the pulsed signal properly and record the results.
8. Repeat steps 4, 5, 6, and 7 at 1 GHz, 3 GHz, 6 GHz, 10 GHz, 12.4 GHz, 15 GHz, 18 GHz, and 20 GHz. For Model 588B counters, change the pulse width from the modulator to 500 ns and test at 22 GHz, 24 GHz, and 26.5 GHz.

BAND 2 AMPLITUDE DISCRIMINATION TEST

Description

This test verifies that the counter will measure accurately the larger of two signals differing in amplitude by 15 dB or more.

Equipment

Sweep generator (Wiltron 6668B)
Sweep generator (Wiltron 6635B)
Spectrum analyzer (Hewlett Packard 8566B)
Power splitter (Hewlett Packard 11667B)

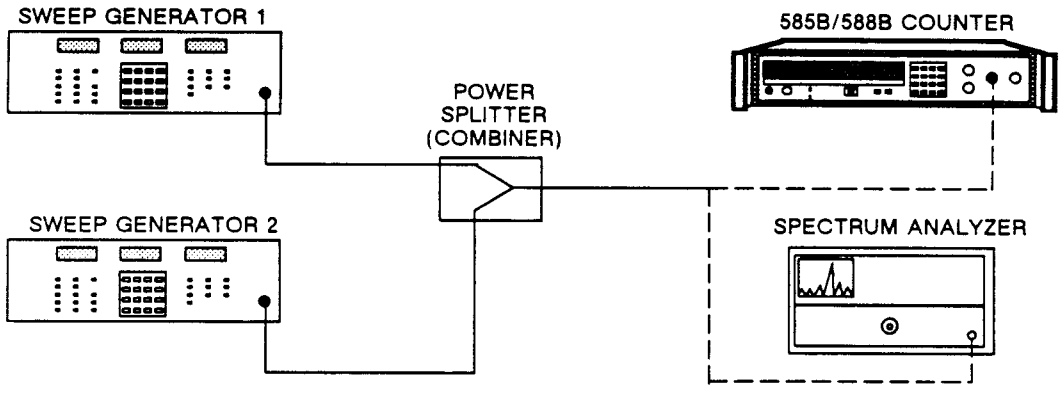

Figure 5-7. Band 2 Amplitude Discrimination Test Setup.

Procedure

1. Connect equipment as shown in Figure 5-7.
2. Set signal generator 1 to 3.0 GHz at 0 dBm and set signal generator 2 to 3.1 GHz at +6 dBm.
3. Using the spectrum analyzer, adjust the generator power levels so that the signal amplitude difference is 15 dB.
4. Verify that the counter correctly measures the frequency of the higher power signal source.
5. Repeat steps 2, 3, and 4 at 6 and 6.1 GHz, at 12 and 12.1 GHz, and at 17.9 and 18 GHz.

BAND 3 SUBBAND 1 RANGE AND SENSITIVITY TEST (588B Option 5804 Only)

Description

This test verifies counter operation from 26.5 GHz to 40 GHz at -20 dBm for both CW and simulated pulsed signals. The pulse generator is used to simulate a pulsed signal by applying a 50 ns ECL low with a 1 MHz repetition rate to the INHIBIT IN connector on the rear panel of the counter. The power meter is used to set signal levels.

Equipment

Sweep generator (Wiltron 6668B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard R8486A)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
Remote sensor (EIP 091)
Cable kit (EIP 590)

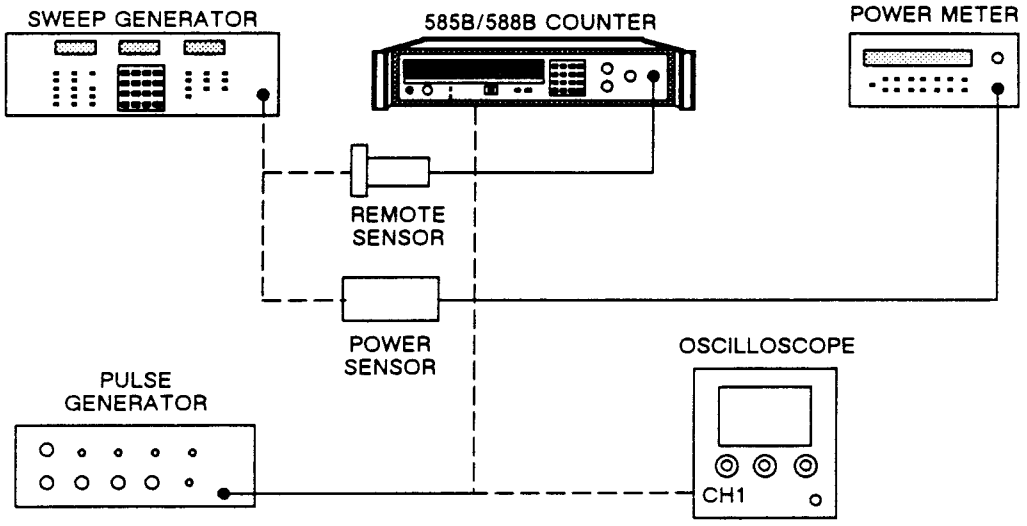

Figure 5-8. Band 3 Range and Sensitivity Test Setup (Model 588B Option 5804 Only).

Procedure

1. Connect equipment as shown in Figure 5-8.
2. Set the counter to Band 3 and select resolution 3.
3. Set the output frequency from the sweeper to 26.5 GHz.
4. Using the power meter, set the output signal level from the sweeper to -20 dBm.
5. Apply the 26.5 GHz signal to the remote sensor, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 30 GHz, 35 GHz, and 40 GHz.
7. Set up the pulse generator to output a 50 ns wide ECL low signal with a 1 MHz repetition rate and apply the signal to the INHIBIT IN connector on the rear panel of the counter. This signal gates signal threshold inside the counter and is used to simulate a pulsed signal.
8. Repeat steps 3, 4, 5, and 6 for the simulated pulsed signal and record the results.

OPERATIONAL TEST RECORD

MODEL_____ SERIAL NO. _____ DATE_____

TEST		ACTUAL		SPECIFICATIONS
INPUT 0 RANGE AND SENSITIVITY TEST				100 Hz TO 250 MHz (CW ONLY)
INPUT SENSITIVITY	100 Hz	_____		-15 dBm
	1 kHz	_____		
	10 kHz	_____		
	100 kHz	_____		
	1 MHz	_____		
	10 MHz	_____		
	100 MHz	_____		
	200 MHz	_____		
	250 MHz	_____		
INPUT 1 RANGE AND SENSITIVITY TEST		CW	PULSE	250 MHz TO 1 GHz
INPUT SENSITIVITY	250 MHz	_____	_____	-15 dBm
	300 MHz	_____	_____	
	400 MHz	_____	_____	
	500 MHz	_____	_____	
	600 MHz	_____	_____	
	700 MHz	_____	_____	
	800 MHz	_____	_____	
	900 MHz	_____	_____	
	1 GHz	_____	_____	
INPUT 2 RANGE AND SENSITIVITY TEST		CW	PULSE	950 MHz TO 20 GHz (26.5 GHz for 588B)
INPUT SENSITIVITY	950 MHz	_____	_____	-20 dBm
	1 GHz	_____	_____	
	3 GHz	_____	_____	
	6 GHz	_____	_____	
	10 GHz	_____	_____	
	12.4 GHz	_____	_____	
	15 GHz	_____	_____	
	18 GHz	_____	_____	
	20 GHz	_____	_____	
588B ONLY	22 GHz	_____	_____	-10 dBm
	24 GHz	_____	_____	
	26.5 GHz	_____	_____	

OPERATIONAL TEST RECORD (Continued)

TEST		ACTUAL		SPECIFICATIONS
INPUT 2 AMPLITUDE DISCRIMINATION TEST				
CONDITIONS: F1 > F2 BY 15 dB OR MORE				
F1	F2	PASS	FAIL	
3 GHz	3.1 GHz	_____	_____	15 dB
6.1 GHz	6 GHz	_____	_____	
12 GHz	12.1 GHz	_____	_____	
18 GHz	17.9 GHz	_____	_____	
BAND 3-1 RANGE AND SENSITIVITY TEST (588B Option 5804 Only)				26.5 GHz TO 40 GHz
		CW	PULSE	
INPUT SENSITIVITY:	26.5 GHz	_____	_____	-20 dBm
	30 GHz	_____	_____	
	35 GHz	_____	_____	
	40 GHz	_____	_____	

SECTION 6
THEORY OF OPERATION

INTRODUCTION

The 585B/588B microwave counters are microprocessor-based multifunction instruments that automatically measure CW and pulse signals. Pulse widths as narrow as 50 ns and pulse periods as short as 250 ns are measured to a resolution of 10 ns, respectively. Using inhibit input, the instruments can profile pulsed or chirped CW signals using gates as narrow as 15 ns. No manual switching is required to measure CW or pulse signals.

The frequency range of the 585B is 100 Hz to 20 GHz. The frequency range of the 588B is 100 Hz to 26.5 GHz and can be extended by option up to 170 GHz. On both instruments the range of the pulse width measurements is from 50 ns to one second and the range of pulse period measurements is 250 ns to one second.

All major functions are controlled through the 21-key, functionally grouped keyboard. Information is output via a 9-digit, sectionalized LED frequency display, a 3-digit floating point LED pulse parameter display, and a 20-message LED annunciator bank.

Microprocessor control and the unique architecture permit not only the major counter functions such as frequency offsets, frequency range limits, and averaging capabilities, but also a variety of special functions such as internal diagnostics, calibration and test aids, and sophisticated operational enhancements.

All front panel controls, except the POWER switch, and all background functions are externally programmable via the IEEE 488-1978 standard GPIB (General Purpose Interface Bus). Additionally, all displayed information, as well as counter setup status, is accessible via the GPIB.

The counter can best be understood by considering its four major sections: the basic counter, the RF converter (Bands 0 and 1), the microwave converter (Band 2), and the optional millimeter wave converter (Band 3). Information on the optional millimeter wave converter is contained in Section 11 of this manual.

BASIC COUNTER

The basic counter, shown in Figure 6-1, receives input signals from all four bands and performs both frequency measurements and pulse parameter measurements (pulse width and pulse period). The basic counter can directly measure the frequency of signals from 100 Hz to 250 MHz.

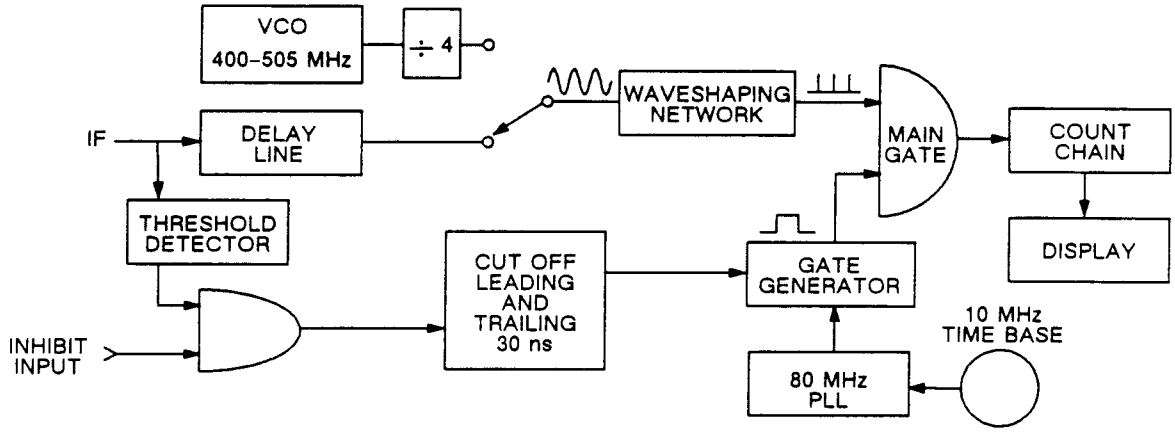

Figure 6-1. Block Diagram of Basic Counter.

Overall operation of the counter is controlled by processor/GPIB assembly, A5. This assembly contains a Motorola 68B09 microprocessor, its control logic, the system memory, and the

circuitry for the GPIB interface. It communicates with all other assemblies in the counter via a triple bus system: the data bus, address bus, and control bus. Each assembly (except for the signal conditioner and gate control board) contains a peripheral interface adapter (PIA) that provides the interface between the bus system and the counter hardware.

Frequency measurements are performed by comparing the unknown signal to a reference frequency, namely the time base. The standard time base is a 10 MHz temperature compensated crystal oscillator (TCXO). Optional high stability ovenized oscillators are also available for improved frequency accuracy. For coherence with system clocks, the counters have the capability of accepting an external 10 MHz reference. To improve performance on pulsed signals, the internal clock is an 80 MHz time base

A frequency measurement is made by generating a time interval (gate time) consisting of a number of cycles of the reference. This gate time is used as an interval during which the input signal is counted by the count chain assembly. This function is considerably more difficult for pulsed signals than it is for CW signals and must be accomplished as two functions. The first is to supply a gate to the count chain that is present only when an input signal is also present. The second is to accumulate the total time during which the gate is applied, until the desired gate time is reached.

The first operation requires that the gate begin after the signal is present at the count chain and end prior to the end of the signal. This is accomplished by generating a gate approximately 30 ns shorter than the RF signal. The arrival time at the count chain of the IF from the converter is then controlled by a delay line so the gate will fall entirely within the IF pulse.

The second operation is accomplished by counting reference clock pulses whenever the gate is open until a total time equal to 1/resolution is obtained. This requires that each gate opening is an exact integral number of clock pulses. Since an 80 MHz clock is being used, the gate will be an exact multiple of 12.5 ns.

Pulse widths are measured by detecting the signal and counting the number of zero crossings of the phase locked VCO signal (prescaled by 4) that occur while the signal is present. The microprocessor then calculates the pulse width by multiplying the number of zero crossings by the period of the VCO signal. Pulse period measurements are made using a similar technique, except that the counter counts zero crossings during the time from the rising edge of one pulse to the rising edge of the next pulse.

RF CONVERTERS

BAND 0 RF CONVERTER (CW ONLY)

Signals between 100 Hz and 250 MHz are counted directly. The gate width is set according to a specified resolution (from resolution 2 to resolution 6). In the 100 Hz resolution mode (resolution 2 or less), the gate width is set to 10 ms by taking ten 1 ms gates. To improve count accuracy, 10 of these 10 ms gates are averaged. The signal threshold detector is set to provide a constant threshold. For this band, the counter continuously counts. If no signal is applied, the counter will gate, but the measurement will be zero.

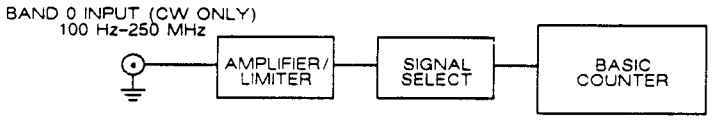

Figure 6-2. Band 0 Block Diagram.

BAND 1 RF CONVERTER

Signals between 250 MHz and 1 GHz are prescaled by four before reaching the basic counter. In this mode, the gate is made four times longer to properly count the prescaled signal. During signal acquisition, the counter monitors the RF detector, and when a signal is detected, the RF gain is adjusted to set the level of the IF 3 dB above threshold and the signal is counted. After every measurement, the RF gain is readjusted to ensure rapid tracking of a moving signal. (See Figure 6-4.)

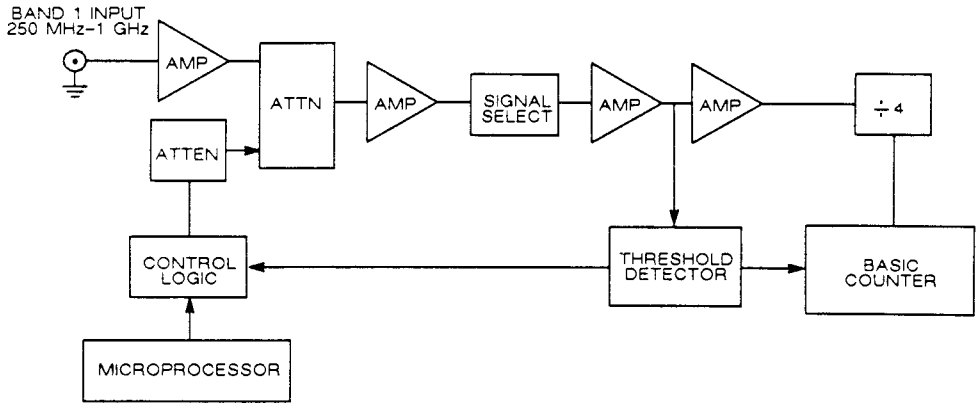

Figure 6-3. Band 1 Block Diagram.

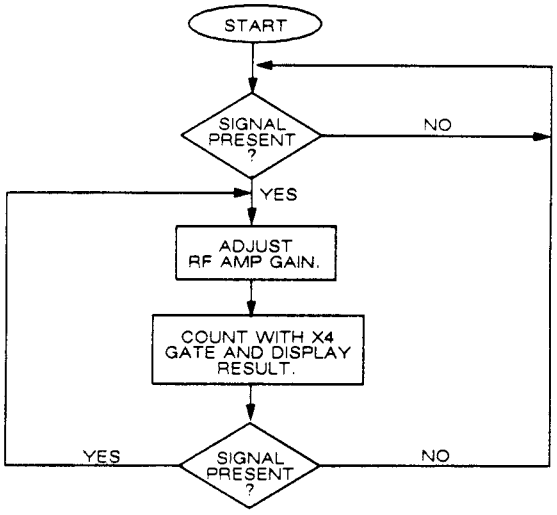

Figure 6-4. Band 1 RF Converter Lock Process Flow Diagram.

BAND 2 MICROWAVE CONVERTER

Frequency measurement in the microwave band is accomplished using a narrow bandpass microwave filter to eliminate all but the desired signal and then downconverting signal to an IF signal of approximately 120 MHz. Figure 6-5 is a block diagram of the Band 2 converter, and Figure 6-6 is a flow diagram showing converter operation.

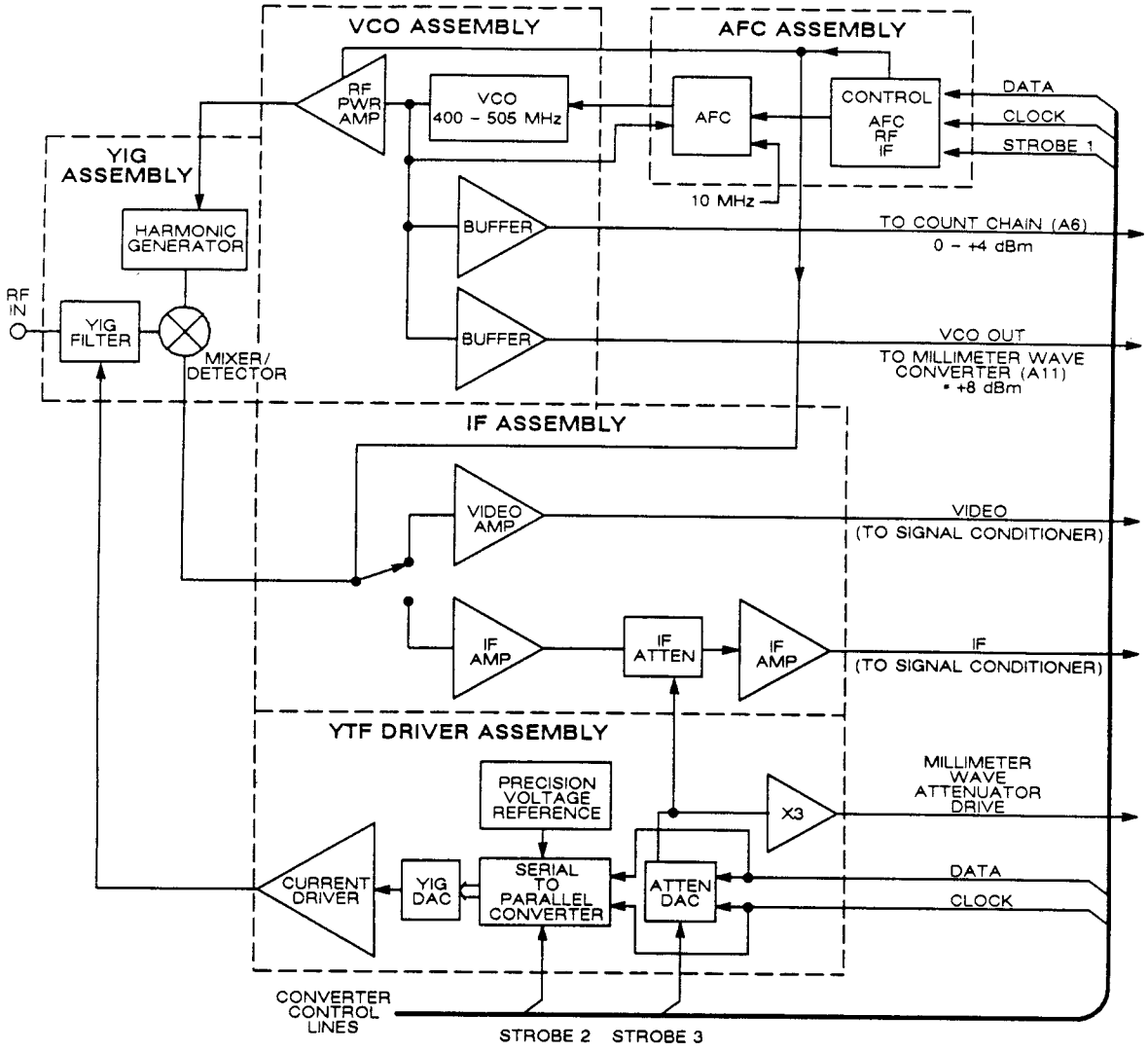

Figure 6-5. Band 2 Microwave Converter Block Diagram.

The actual process of signal measurement in the microwave band is accomplished using a series of steps:

1. Search for the largest signal.
2. Center the YIG on the largest signal.
3. Calculate the harmonic number and required VCO frequency.
4. Adjust the IF gain.
5. Measure the IF.
6. Perform calculations.
7. Display measurement.

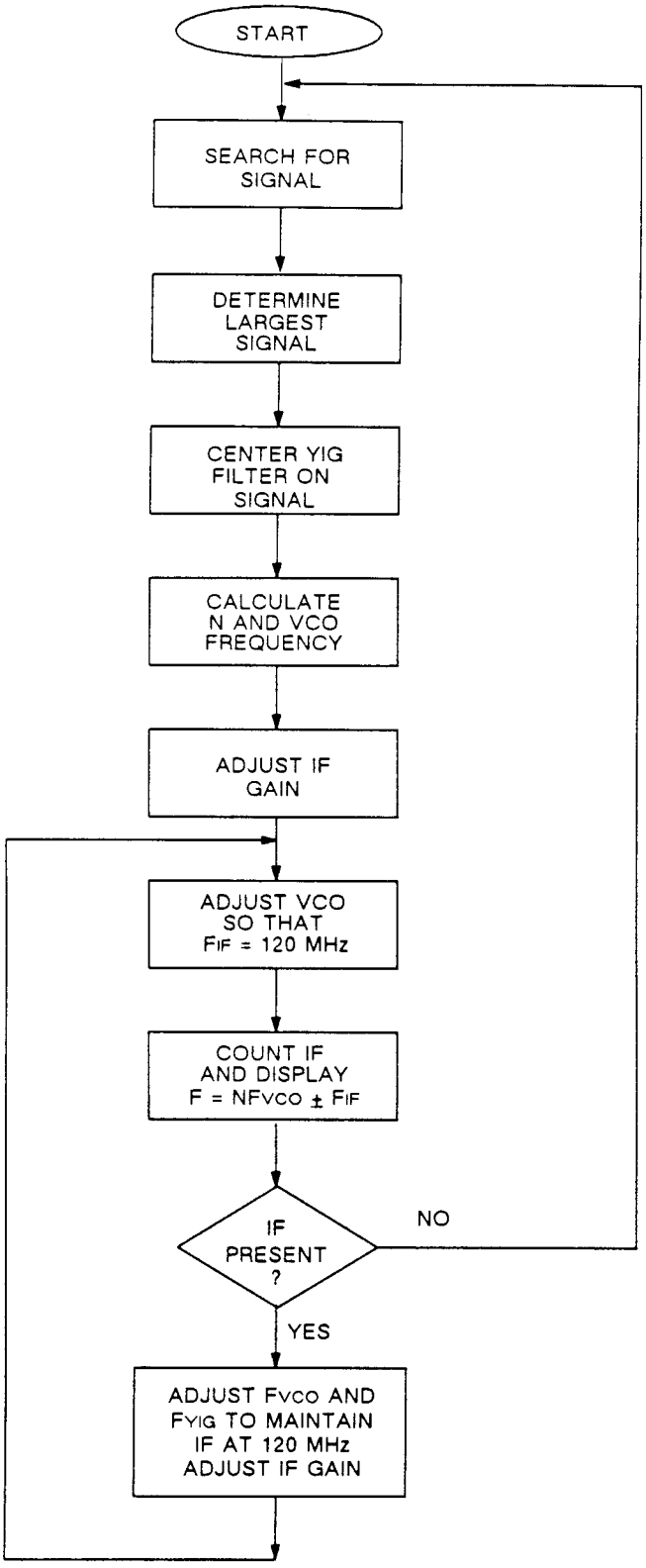

Figure 6-6. Microwave Converter Operation Flow Diagram.

During the search routine the counter selects the largest signal present within the selected, or default, range of the Band 2 input. During this routine, the electronically tunable microwave bandpass YIG filter is being continuously stepped from its low to high limits. The output from the YIG filter is applied to the mixer, which is used as an RF detector. The output from the mixer is applied to the video amplifier which feeds a flash A/D converter, with a resolution of approximately 5 dB. When the counter detects a signal, the YIG DAC setting and relative amplitude of the signal (output from the flash A/D) is stored in memory, and the search routine continues. If other signals are detected, their relative amplitudes are compared with the stored information. If the new signal is higher in amplitude, the memory is updated with information on the new signal. After searching the entire band, the YIG DAC setting and relative amplitude of the highest signal present are stored in memory.

The next step is to precisely center the YIG on the selected signal. This process begins by moving the YIG to the signal selected during the search routine. The YIG is then stepped in 2 MHz steps around the signal until four points are found: the points on either side of the peak 1.25 dB down from the peak and the points on either side of the peak 5 dB down from the peak. From these points the approximate "center of mass frequency" of the signal is found, and the YIG filter is set to that frequency. The "center of mass" algorithm compensates for pulsed signals that deviate from perfect sinX/X shape and for nonsymmetries in the YIG filter.

After the YIG is centered on the signal, the harmonic number N is calculated based on the setting of the YIG filter using the following formula:

$$N = \frac{F_{YIG} - 120\ MHz}{500\ MHz}$$

The resulting N is rounded up to the next higher integer. At this point low side mixing is assumed, and the proper VCO frequency is calculated using the formula:

$$F_{VCO} = \frac{F_{YIG} - 120\ MHz}{N}$$

If the results yield a VCO frequency which is less than 400 MHz (the minimum VCO frequency), high side mixing is assumed, and FVCO is recalculated using the formula:

$$F_{VCO} = \frac{F_{YIG} + 120\ MHz}{N}$$

At this point the IF gain is adjusted to set the signal level approximately 3 dB above signal threshold.

Since FYIG is only approximately equal to FIN, the frequency will not be exactly 120 MHz. Therefore, the next step is to adjust the VCO to shift FIN into the middle of the IF passband by counting FIF and adjusting FVCO as follows:

$$\Delta F_{VCO} = \frac{\pm F_{IF} - 120\ MHz}{N}$$

Where: -FIF is used if high side mixing and
+FIF is used if low side mixing.

Once the VCO corrections have been made, the counter counts the IF and calculates the input frequency using the following formula:

$$F_{IN} = N \times F_{VCO} \pm F_{IF}$$

Where: N = Harmonic number
F_{VCO} = VCO frequency
$\pm$ = + for low side mixing
– for high side mixing

and the results are displayed.

After each measurement, new frequencies for the YIG and VCO are calculated to maintain the IF at 120 MHz, and the IF gain is readjusted to keep the signal 3 dB above threshold. This method provides rapid tracking of a signal being tuned.

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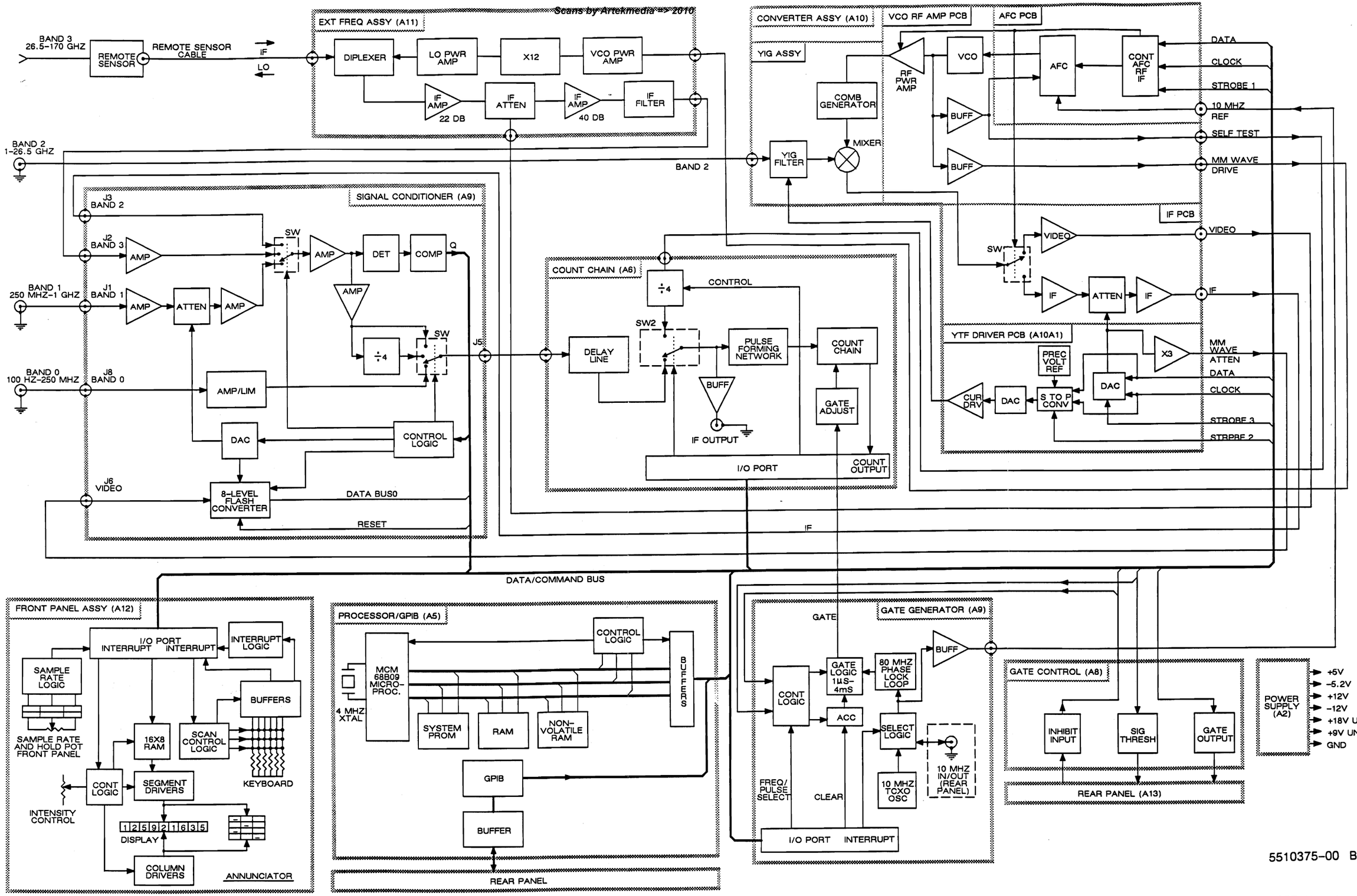

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Figure 6–7. Model 585B/588B Counters Functional Block Diagram.

SECTION 7
ADJUSTMENT AND CALIBRATION

INTRODUCTION

The following adjustment and calibration procedures for the EIP 585B/588B counters should be performed every 12 months, to maintain counter accuracy. However, depending upon the required accuracy, the procedures may be performed at more frequent intervals. For sample calculations of counter measurement accuracy using calibration intervals of both 6 and 12 months, refer to page 3-18. In addition, further adjustments within each calibration interval should be made if the counter does not operate as specified, or if it has been repaired. If the adjustments or calibrations do not result in the specified performance, refer to the troubleshooting section of this manual.

The adjustment and calibration procedure comprises the following:

1. Power supply adjustment
2. Display intensity adjustment
3. Time base calibration
4. Band 2 YIG DAC automatic calibration (Special Function 91)
5. Gate error calibration (Special Function 92)

All adjustments and calibrations require removal of the top cover. The display intensity adjustment is for user comfort only.

Table 7-1 describes the functions, specifications, and methods to be used when performing the adjustment and calibration routines. Figure 7-1 shows the location of the adjustment controls.

Table 7-1. Adjustment and Calibration Procedures.

Function	Performance Specification	Method
Power supply adjustment	Voltage between A2TP1 (+12 V) and ground is +12 ±0.05 V	Adjust A2R3; check with DVM.
	Voltage between A2TP2 (-12 V) and ground is -12 ±0.05 V	Adjust A2R6; check with DVM.
Time base adjustment	Adjust the output frequency of the TCXO to 10 MHz ±1 Hz	Turn the TCXO calibration screw, check count output using 545B counter with external time base standard (e.g., WWV).
YIG DAC automatic calibration	Automatic calibration of DAC to YIG filter	Use Special Function 91.
Gate error calibration	Gate error is ≤ ±0.05 times the gate width	Use Special Function 92 to calibrate gate accuracy in each band.
Display intensity	LED brightness level is adjusted to suit operator's comfort	Adjust A12A2R4 on front panel logic board.

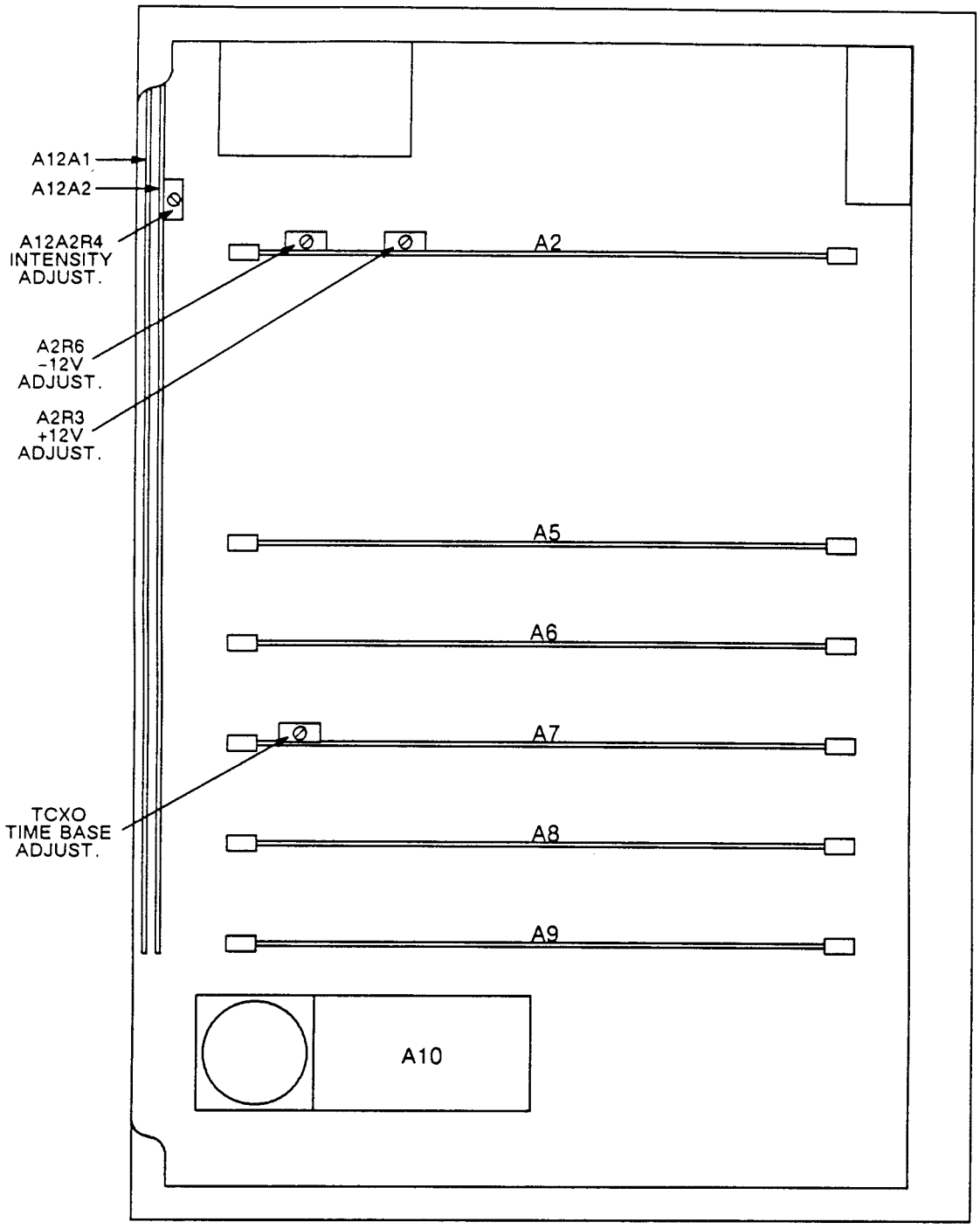

Figure 7-1. Adjustment Control Locations.

EQUIPMENT REQUIRED

Minimum use specifications are the principle parameters required for calibration and are included to assist in selecting alternative equipment. Satisfactory performance of alternative equipment should be verified prior to use. All applicable equipment must bear evidence of current calibration.

Table 7-2. Equipment Required.

Description	Critical Parameters	Recommended Manufacturer	Model
Microwave counter	0.1 Hz resolution	EIP	545B
Digital voltmeter	4 1/2 digit resolution	Fluke	8050A
Pulse generator	20 ns pulses	Wavetek	801
50 ohm feedthrough termination	50 ohms resistance	Pamona	4119-50
Oscilloscope	100 MHz bandwidth	Tektronix	475
Synthesized sweeper	250 MHz to 26.5 GHz	HP	8340B
Power meter	250 MHz to 26.5 GHz	HP	436A
Power sensor	250 MHz to 26.5 GHz	HP	8484A
Frequency standard	Short-term stability $\geq 1 \times 10^{-11}$	Stanford Research Systems	FS700 with Option 01

PRELIMINARY OPERATIONS

COVER REMOVAL

All of the adjustment and calibration procedures described in this section require removal of the top cover of the counter. To remove the cover, proceed as follows:

1. Remove the 12 screws from the top cover.
2. From the rear of the counter, insert a flat blade screwdriver (or equivalent tool) into one of the 5/16-inch holes located on the upper portion of the rear frame assembly.
3. Gently push upward to dislodge the top cover.

WARNING

Whenever the instrument cover is removed, components that carry high voltages are exposed. To avoid personal injury, extreme caution should be exercised. Only a qualified technician who is aware of the hazards involved should perform the following adjustment and calibration procedures.

MEMORY PROTECT FEATURE

In order to prevent accidental alteration or erasure of calibration data stored in nonvolatile RAM, a memory protect feature is included on the Processor/GPIB assembly (A5). Before Special Function 46 (display/alter memory), 76 (EEPROM test), 91 (YIG DAC calibration), or 92 (gate accuracy calibration) can be activated, this memory protect feature must first be disabled. Therefore, to activate Special Functions 46, 76, 91, or 92, perform the following:

1. Turn the POWER switch of the 585B/588B to STBY.
2. Remove the top cover of the counter.
3. Refer to the Processor/GPIB component locator on page 10-30 and install a jumper on PCB assembly A5, as shown, to disable the memory protect.
4. Turn the POWER switch to ON.
5. Activate the desired special function.
6. After completion of the special function, turn the POWER switch to STBY.
7. Remove the jumper installed on A5, in step 3 above, to re-enable the memory protect.
8. Replace the top cover of the counter.
9. Turn the POWER switch to ON.

ADJUSTMENTS

WARNING

Whenever the instrument cover is removed, components that carry high voltages are exposed. To avoid personal injury, extreme caution should be exercised. Only a qualified technician who is aware of the hazards involved should perform the following adjustment and calibration procedures.

POWER SUPPLY ADJUSTMENT

Equipment Required

Digital voltmeter (Fluke 8050A)

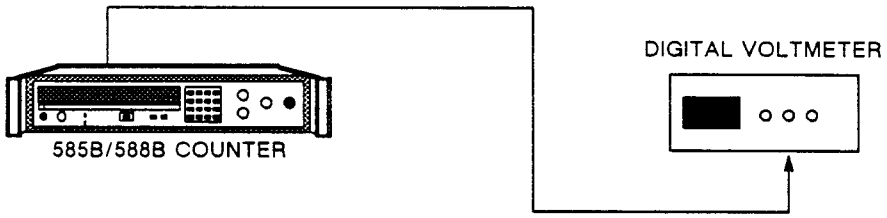

Figure 7-2. Power Supply Adjustment Setup.

Procedure

1. Set up equipment as shown in Figure 7-2 and described below.
2. Remove the top cover of the counter.
3. Turn counter on and let it warm up for 30 minutes.
4. Connect the digital voltmeter between TP1 (+12 V) on PCB A2 and ground.
5. Check that the voltage reading is +12 V ±0.05 V. If not, adjust R3 until the voltage measures +12.00 ±0.05 V.
6. Connect the DVM between TP2 (-12 V) on PCB A2 and ground.
7. Check that the voltage reading is -12 V ±0.05 V. If not, adjust R6 until the voltage measures -12.00 ±0.05 V.

DISPLAY INTENSITY ADJUSTMENT

1. Remove top cover of the counter.

2. Adjust display intensity potentiometer R4 on PCB A12A2 for most comfortable viewing.

CALIBRATION

TIME BASE CALIBRATION

The time base oscillator used in either counter is a 10 MHz, temperature compensated crystal oscillator (TCXO). The accuracy of this oscillator directly affects the measurement accuracy of the counter. From the time an oscillator is set to its specified frequency it will begin drifting, and the magnitude of this drift is specified as the aging rate of the oscillator. Time base calibration compensates for this drift and should be performed at least every 12 months.

The procedure described herein uses an EIP Model 545B Microwave Frequency Counter to measure the frequency of the time base. The 545B was chosen because it provides a 0.1 Hz resolution in Band 1. The external reference input on the 545B must be connected to a 10 MHz frequency standard, the accuracy of which should be several orders of magnitude better than the TCXO.

Equipment Required

Microwave counter (EIP 545B)
50 ohm feedthrough termination (Pamona 4119-50)
10 MHz frequency standard (Stanford Research Systems FS700)

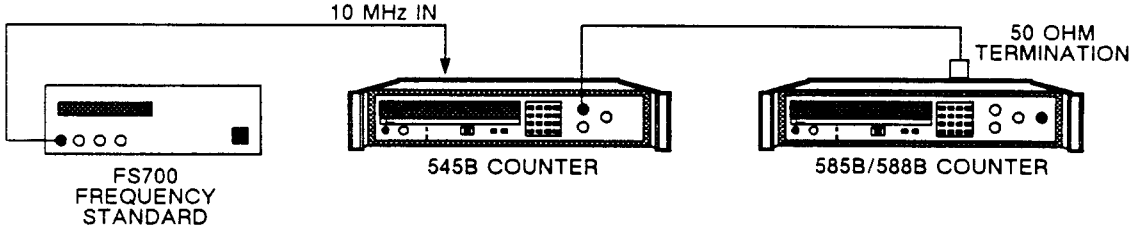

Figure 7-3. Time Base Calibration Setup.

Procedure

1. Set up equipment as shown in Figure 7-3 and described below.

2. Remove the top cover of the counter.

3. Turn counter on and allow it to warm up for 30 minutes.

4. Connect the 10 MHz IN/OUT connector on the rear panel of the 585B/588B through a 50 ohm feedthrough termination to the BAND 1 input of an EIP 545B counter. Select 0.1 Hz resolution on the 545B by pressing the RES key followed by the decimal point key and then the 1 key.

5. Connect a 10 MHz frequency standard to the 10 MHz IN/OUT (external reference) connector on the rear panel of the 545B counter. On the 545B counter, set the rear panel 10 MHz INT/EXT switch to EXT.

6. Set the 585B/588B TCXO frequency control (on gate generator PCB A7) to 10 MHz ±1 Hz by turning the adjustment screw located on the top of the TCXO case (see Figure 7-1) and observe that the 545B counter displays 10 MHz ±1 Hz.

YIG DAC AUTOMATIC CALIBRATION - SPECIAL FUNCTION 91

The counter uses an electronically tunable microwave bandpass YIG filter on the BAND 2 input. The frequency to which the filter is tuned is controlled by a digital-to-analog converter (DAC). The YIG DAC calibration develops a table of correction factors that correlates the digital information sent to the DAC to the frequency to which the YIG filter is tuned.

When this calibration function is activated, the counter displays "F1" and measures a user-supplied 2 GHz input. It then displays "F2," waits for the user to press the TRIG key indicating the frequency has been changed to 18 GHz, and measures it. The counter then calculates and stores (in nonvolatile memory) the correction factors for the YIG DAC.

CAUTION

Care must be used when operating Special Function 91. Although the counter cannot be damaged by this function, improper operation of it can affect the counter calibration, possibly rendering the counter unusable until it can be recalibrated. Do not call this function unless familiar with its operation.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)

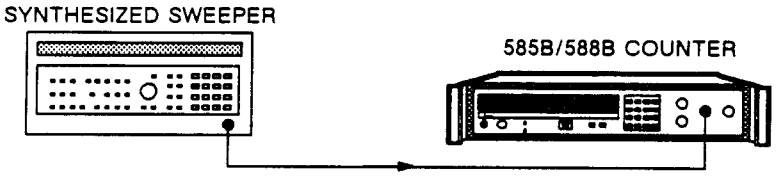

Figure 7-4. YIG DAC Automatic Calibration Setup.

Procedure

1. Remove the top cover of the counter.
2. Disable the memory protect feature (see page 7-3).
3. Apply a 2 GHz signal at approximately 0 dBm to BAND 2 input connector.
4. Press keys for Special Function 91. When the counter displays "F1," press TRIG key.
5. When the display changes from "F1" to "F2," apply an 18 GHz signal at approximately 0 dBm and press TRIG key.
6. When the display returns to normal, the YIG DAC is calibrated.

GATE ERROR CALIBRATION - SPECIAL FUNCTION 92

This adjustment reduces the gate error. When narrow pulses are counted, the gate is opened and closed many times in order to accumulate enough gate time to provide the required

resolution. Each time the gate opens and closes, there is a small but measurable error. The total error is proportional to the number of times the gate is cycled during a measurement, and is inversely proportional to the gate width. This error is also related to both temperature and input frequency.

In the EIP 585B/588B counters, the worst case gate error, including all variables, is specified as:

BAND 1: Gate Error = ±0.07/GW
BAND 2: Gate Error = ±0.01/GW

where GW in seconds is the logical AND of the pulse width and the inhibit signal minus 30 ns.

Performing this adjustment at room temperature (25 °C) guarantees performance to specifications over the temperature range of the counter. If the counter is to be used at a temperature other than 25 °C, performance may be improved by performing this calibration at that temperature.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse generator (Wavetek 801)
50 ohm feedthrough termination (Pamona 4119-50)
Oscilloscope (Tektronix 475)

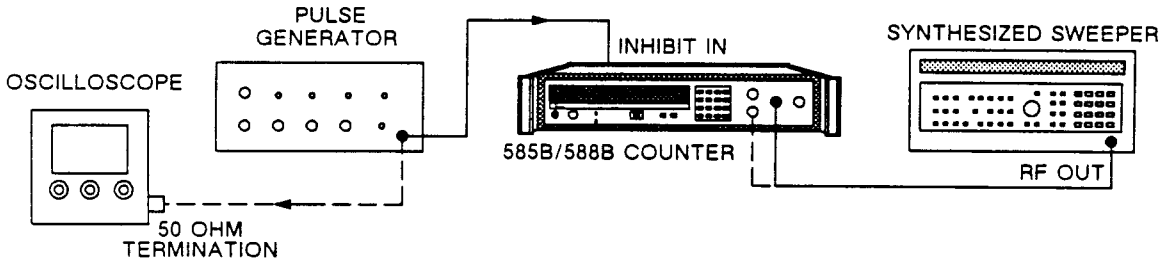

Figure 7-5. Bands 1 and 2 Gate Error Calibration Setup.

Procedure (BAND 1 Gate Error Calibration)

1. Remove the top cover of the counter.
2. Disable the memory protect feature (see page 7-3).
3. Set up equipment as shown in Figure 7-5 and described below.
4. Select BAND 1. Apply a 650 MHz, 0 dBm CW signal from the microwave synthesizer to the BAND 1 input connector.
5. Connect the pulse generator to the oscilloscope through a 50 ohm termination at the oscilloscope. Set the pulse generator as follows: 1 MHz PRF, 50 ns complementary pulse width, base line at 0 V, and amplitude at -1 V. Connect the pulse generator to the INHIBIT INPUT connector on the rear panel of the counter.

6. Press keys for Special Function 92, then press TRIG key. The counter display reads SPECIAL 92 and remains in the autocalibrate state for about 2 minutes. At the completion of autocalibration, normal display function resumes.

Procedure (BAND 2 Gate Error Calibration)

1. Remove the top cover of the counter.

2. Disable the memory protect feature (see page 7-3).

3. Set up equipment as shown in Figure 7-5 and described below.

4. Select BAND 2. Apply a 2 to 10 GHz, 0 dBm CW signal from the microwave synthesizer to the BAND 2 input connector.

5. Connect the pulse generator to the oscilloscope through a 50 ohm termination at the oscilloscope. Set the pulse generator as follows: 1 MHz PRF, 50 ns complementary pulse width, base line at 0 V, and amplitude at -1 V. Connect the pulse generator to the INHIBIT IN connector on the rear panel of the counter.

6. Press keys for Special Function 92, then press TRIG key. The counter display reads SPECIAL 92 and remains in the autocalibrate state for about 2 minutes. At the completion of autocalibration, normal display function resumes.

SECTION 8
PERFORMANCE VERIFICATION TESTS

INTRODUCTION

This section describes the performance verification test procedures for the EIP Models 585B and 588B Pulsed Microwave Frequency Counters. Test methods are summarized in Table 8-1.

Table 8-1. Performance Verification Test Methods.

Counter Characteristic	Performance Specifications	Test Method
Frequency Range		
Band 0		
100 Hz to 250 MHz	Counter accurately measures over entire range.	Checked by verifying that counter displays accurate reading of frequency input from synthesized signal generator.
Band 1		
250 MHz to 1 GHz	Counter accurately measures over entire range.	Checked by verifying that counter displays accurate reading of frequency input from synthesized signal generator.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Counter accurately measures over entire range.	Checked by verifying that counter displays accurate reading of frequency input from synthesized signal generator.
Sensitivity		
Band 0		
100 Hz to 250 MHz	-15 dBm	Checked by verifying that counter set to resolution 3 displays a measurement within 1 kHz of signal input from signal generator at -15 dBm.
Band 1		
250 MHz to 1 GHz	-15 dBm	Checked by verifying that counter set to resolution 3 displays a measurement within 1 kHz of signal input from signal generator at -15 dBm.
Band 2		
950 to 20 GHz 20 to 26.5 GHz (Model 588B)	-20 dBm -10 dBm	Checked by verifying that the counter displays a reading within 1 kHz of signal input from signal generator at specified power level.

Table 8-1. Performance Verification Test Methods. (Continued)

Counter Characteristic	Performance Specifications	Test Method
Maximum Input		
Band 0		
100 Hz to 250 MHz	+7 dBm	Checked by verifying that the counter displays a measurement within 1 kHz of input signal at maximum power level.
Band 1		
250 MHz to 1 GHz	+7 dBm	Checked by verifying that the counter displays a measurement within 1 kHz of input signal at maximum power level.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	+7 dBm	Checked by verifying that the counter displays measurement within 1 kHz of input signal at maximum power level.
Amplitude Discrimination		
Band 1		
250 MHz to 1 GHz	10 dB	Checked by verifying that counter measures the higher power signal of two signals input from signal generators.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	15 dB 15 dB	Checked by verifying that counter measures the higher power signal of two signals input from signal generators.
Gate Error		
Band 1		
250 MHz to 1 GHz	Gate Error (in Hz) = $\pm$0.07/ Gate Width	Checked by verifying that the counter displays measurement within the limits of the gate error when appropriate inhibit input and signal are applied.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Gate Error (in Hz) = $\pm$ 0.01/ Gate Width	Checked by verifying that the counter displays measurement within the limits of the gate error when appropriate inhibit input and signal are applied.

Table 8-1. Performance Verification Test Methods. (Continued)

Counter Characteristic	Performance Specifications	Test Method
Distortion Error		
Band 1		
250 MHz to 1 GHz	Distortion Error (in Hz) = ± 0.03/ Pulse Width (in seconds) - 3×10^{-8}	Checked by calculating the distortion error by subtracting the gate error from the frequency of a pulsed signal input from a signal generator and verifying that it falls within the specification.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Distortion Error (in Hz) = ± 0.03 Pulse Width (in seconds) - 3×10^{-8}	Checked by calculating the distortion error by subtracting the gate error from the frequency of a pulsed signal input from a signal generator and verifying that it falls within the specification.
Averaging Error		
Band 1		
250 MHz to 1 GHz	Averaging Error = $\pm(2)\sqrt{[RES / (GW)(AVG)^*}$	Checked by using the displayed frequency of a number of measured pulsed signals input from a signal generator to calculate the sample variance and then verifying that it is within the specified limits.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Averaging Error = $\pm\sqrt{[RES / (GW)(AVG)^*}$	Checked by using the displayed frequency of a number of measured pulsed signals input from a signal generator to calculate the sample variance and then verifying that it is within the specified limits.
Frequency Limits		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Instrument will ignore signals greater than 100 MHz outside the specified limit at 10 MHz resolution ± 50 MHz accuracy.	Checked by applying a signal 70 MHz from the entered frequency, and verifying that it is not read, and applying a signal 50 MHz from the entered frequency, and verifying that it is read.

* RES is the specified instrument resolution in Hz (This is true up to 1 MHz resolution. Above 1 MHz resolution RES = 10^6 Hz.) GW in seconds is the logical AND of inhibit and pulse width minus 3×10^{-8} seconds. AVG is the number of specified count average.

Table 8-1. Performance Verification Test Methods. (Continued)

Counter Characteristic	Performance Specifications	Test Method
Center Frequency		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Counter locks a signal ±50 MHz from entered frequency at 10 MHz resolution.	Checked by applying a signal 70 MHz from the entered frequency, and verifying that it is not read, and applying a signal 50 MHz from the entered frequency, and verifying that it is read.
Maximum Video		
Band 1		
250 MHz to 1 GHz	Counter maintains accuracy in presence of video signal 20 dB or more below RF signal.	Checked by applying a video pulse to the inhibit input and verifying that it does not change the accuracy of the counter reading.
Band 2		
950 MHz to 20 GHz 950 MHz to 26.5 GHz (Model 588B)	Counter maintains accuracy in presence of video signal 20 dB or more below RF signal.	Checked by applying a video pulse to the inhibit input and verifying that it does not change the accuracy of the counter reading.

EQUIPMENT REQUIREMENTS

Equipment required for performing performance tests on the EIP Models 585B and 588B counters is listed in Table 8-2.

NOTE

Minimum use specifications are the principal parameters required for performance of the procedures and are included to assist in the selection of alternate equipment. Satisfactory performance of alternate items should be verified prior to use. All applicable equipment must bear evidence of current calibration.

Table 8-2. Recommended Equipment Requirements.

Equipment	Range	Recommended Manufacturer	Model
Synthesized sweeper (2)	10 MHz to 26.5 GHz	Hewlett Packard	8340B
Frequency synthesizer	100 Hz to 10 MHz	Hewlett Packard	3325A
Sweep generator	3 to 18 GHz	Wiltron	6635B
Spectrum analyzer	100 Hz to 22 GHz	Hewlett Packard	8566B

Table 8-2. Recommended Equipment Requirements. (Continued)

Equipment	Range	Recommended Manufacturer	Model
Power meter	10 MHz to 26.5 GHz	Hewlett Packard	437B
Power sensor	10 MHz to 18 GHz	Hewlett Packard	8481A
Power sensor	50 MHz to 26.5 GHz	Hewlett Packard	8485A
Oscilloscope	DC to 100 MHz	Tektronix	475
Power splitter	10 MHz to 26.5 GHz	Hewlett Packard	11667B
Directional coupler	10 to 1000 MHz	Anzac	CH132
Directional coupler	950 MHz to 18 GHz	Narda	4222-16
Directional coupler	18 to 26.5 GHz	Narda	4017C-10
Bidirectional coupler	10 dB	Narda	3022
Pulse generator (2)	5 Hz to 50 MHz	Wavetek	801
Pulse modulator	800 MHz to 2 GHz	Hewlett Packard	8731B
Pulse modulator	2 to 18 GHz	Hewlett Packard	11720A
Pulse modulator	18 to 26.5 GHz	Narda	S214DS
Low attenuation coaxial cable (3)		Gore	P2S01S01036.0
6 dB attenuator (2)	DC to 1 GHz	Texscan	FP-50
3 dB attenuator (3)	DC to 26.5 GHz	Weinschel	9-3
Detector	10 MHz to 18 GHz	Hewlett Packard	8473B
50 ohm termination		Pomona	4119-50

SPECIAL EQUIPMENT

Because of the lack of adequate equipment for testing narrow pulses below 0.8 GHz, a special 0.25 to 1 GHz modulator must be fabricated to test the counter accurately in these ranges. In cases where full capability testing is not necessary, the instrument may be tested using substitute equipment. The pulsed modulator shown in Figure 8-1 can be used for testing Band 1 pulsed capabilities. If it is not necessary to test pulse widths of less than 100 ns, the pulse modulation capabilities of the HP 8340B will be sufficient to test the counter. If another modulator is used, extreme care must be taken to prevent phase distortion of the pulse by the modulator.

All resistors are in ohms.
Double balanced mixer is Mini Circuits TFM-2.

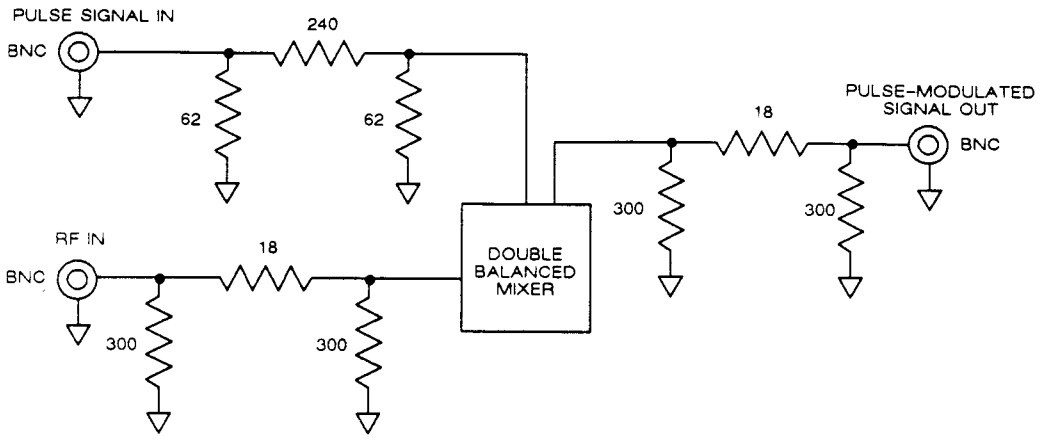

Figure 8-1. Pulse Modulator.

TEST PROCEDURES

NOTE

Review the entire procedure before starting the verification testing process. Verify that the line voltage selector is properly set for the intended single-phase line voltage. Connect the instrument to local line voltage before starting any test.

BAND 0 RANGE/SENSITIVITY TESTS (CW ONLY)

Description

This test verifies counter operation from 100 Hz to 250 MHz at -15 dBm (0.1125 V p-p into 50 ohms) and +7 dBm. The oscilloscope is used to set up signal levels below 10 MHz and the power meter is used to set signal levels at 10 MHz and above. Test setup 1 tests the counter from 100 Hz to 10 MHz, and test setup 2 tests the counter from 10 MHz to 250 MHz.

Equipment Required

Frequency synthesizer (Hewlett Packard 3325A)
Synthesized sweeper (Hewlett Packard 8340B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Power splitter (Hewlett Packard 11687B)
Oscilloscope (Tektronix 475)
50 ohm termination (Pamona 4119-50)

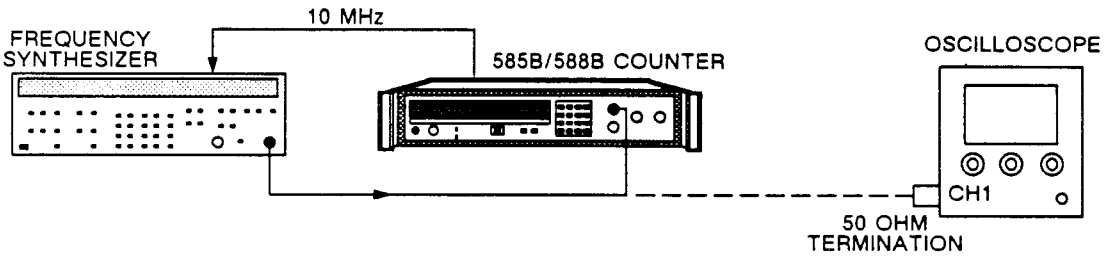

Figure 8-2. Band 0 Range and Sensitivity Test Setup (100 Hz to 10 MHz).

Procedure (100 Hz to 10 MHz)

1. Connect equipment as shown in Figure 8-2.
2. Set 585B/588B counter to Band 0 and select resolution 2.
3. Set output frequency from synthesizer to 100 Hz.
4. Using oscilloscope, set output signal level from synthesizer to -15 dBm (0.11 V p-p into 50 ohms).
5. Apply 100 Hz signal to 585B/588B counter and verify proper reading.
6. Repeat steps 3, 4, and 5 at 1 kHz, 10 kHz, and 100 kHz and at 1 MHz and 10 MHz.
7. Repeat steps 3 through 6 at input power of +7 dBm.

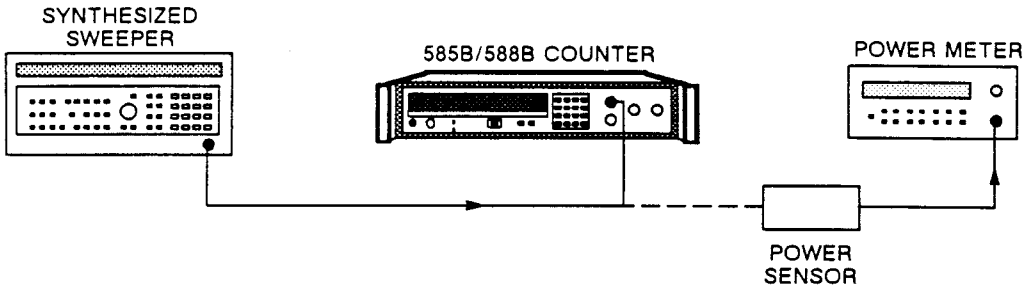

Figure 8-3. Band 0 Range and Sensitivity Test Setup (100 MHz to 250 MHz).

Procedure (100 MHz to 250 MHz)

1. Connect equipment as shown in Figure 8-3.
2. Set 585B/588B counter to Band 0 and select resolution 3.
3. Set synthesizer to 100 MHz.
4. Using power meter, set output signal level from synthesizer to -15 dBm.
5. Apply 100 MHz signal to 585B/588B counter and verify proper reading.
6. Repeat steps 3, 4, and 5 at 200 MHz and 250 MHz.
7. Repeat steps 3 through 6 at input power of +7 dBm.

BAND 1 RANGE/SENSITIVITY TESTS

Description

This test verifies counter operation from 250 MHz to 1 GHz at -15 dBm and +7 dBm for CW signals.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Power splitter (Hewlett Packard 11667B)

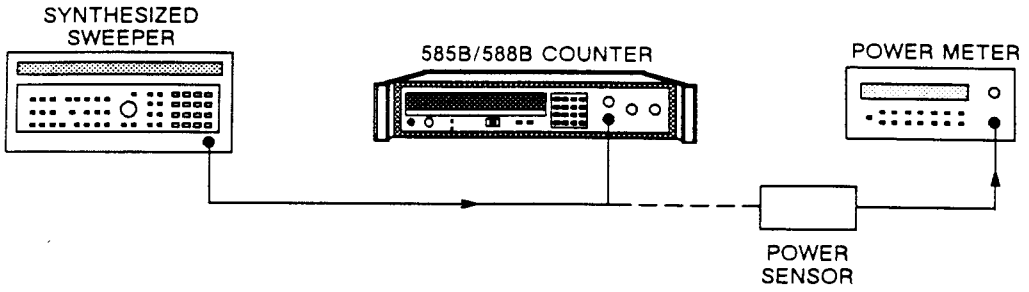

Figure 8-4. Band 1 Range and Sensitivity Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-4.
2. Set 585B/588B counter to Band 1 and select resolution 3.
3. Set synthesizer to 250 MHz.
4. Using power meter, set output signal level from synthesizer to -15 dBm.
5. Apply 250 MHz signal to 585B/588B counter and verify proper reading.
6. Repeat steps 3, 4, and 5 at 300 MHz, 400 MHz, 500 MHz, 600 MHz, 700 MHz, 800 MHz, 900 MHz, and 1 GHz.
7. Repeat steps 3 through 6 at an input power of +7 dBm.

BAND 2 RANGE/SENSITIVITY TESTS

Description

This test verifies counter operation from 950 MHz to 20 GHz at -20 dBm (and from 20 GHz to 26.5 GHz at -10 dBm for the 588B) and +7 dBm for all CW signals.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8485A)
Power splitter (Hewlett Packard 11667B)

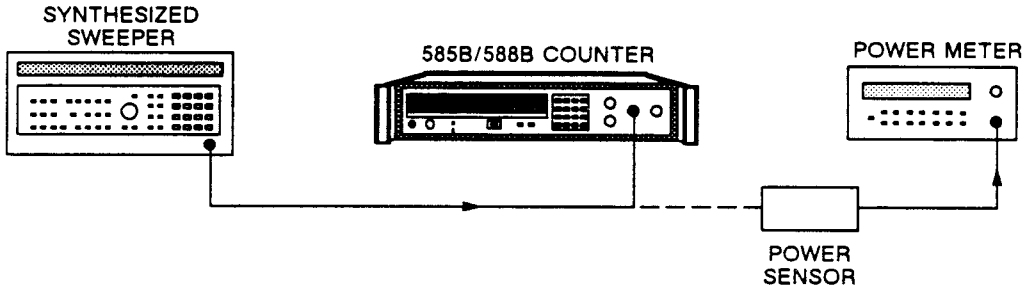

Figure 8-5. Band 2 Range and Sensitivity Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-5.
2. Set 585B/588B counter to Band 2 and select resolution 3.
3. Set synthesizer to 950 MHz.
4. Using power meter, set output signal level from synthesizer to -20 dBm.
5. Apply 950 MHz signal to 585B/588B counter and verify proper reading.
6. Repeat steps 3, 4, and 5 at 1 GHz, 3 GHz, 6 GHz, 10 GHz, 12.4 GHz, 15 GHz, 18 GHz, and 20 GHz. For 588B counters also test at 20 GHz, 22 GHz, 24 GHz, and 26.5 GHz at -10 dBm.
7. Repeat steps 3 through 6 at the input power of +7 dBm.

BAND 1 AMPLITUDE DISCRIMINATION TEST

Description

This test verifies that the counter will measure accurately the larger of two signals differing in amplitude by 10 dB or more.

Equipment Required

Synthesized sweeper (2) (Hewlett Packard 8340B)
Spectrum analyzer (Hewlett Packard 8566B)
Power splitter (Hewlett Packard 11667B)

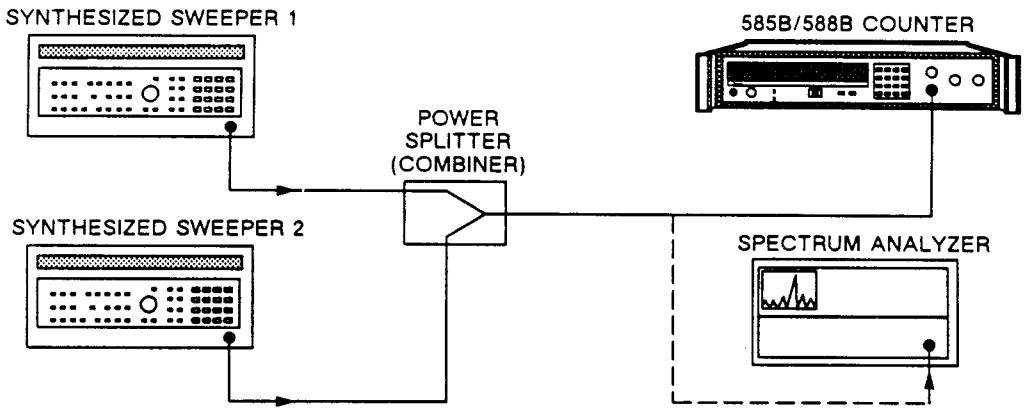

Figure 8-6. Band 1 Amplitude Discrimination Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-6.
2. Set synthesized sweeper 1 to 300 MHz at 0 dBm and set synthesized sweeper 2 to 400 MHz at -10 dBm.
3. Verify that 585B/588B counter correctly measures the frequency of the high power signal source

4. Repeat steps 2 and 3 at 600 MHz, 700 MHz, 900 MHz, and 1 GHz.

BAND 2 AMPLITUDE DISCRIMINATION TEST

Description

This test verifies that the counter will measure accurately the larger of two signals differing in amplitude by 15 dB or more.

Equipment Required

Synthesized sweeper (2) (Hewlett Packard 8340B)
Spectrum analyzer (Hewlett Packard 8566B)
Power splitter (Hewlett Packard 11667B)

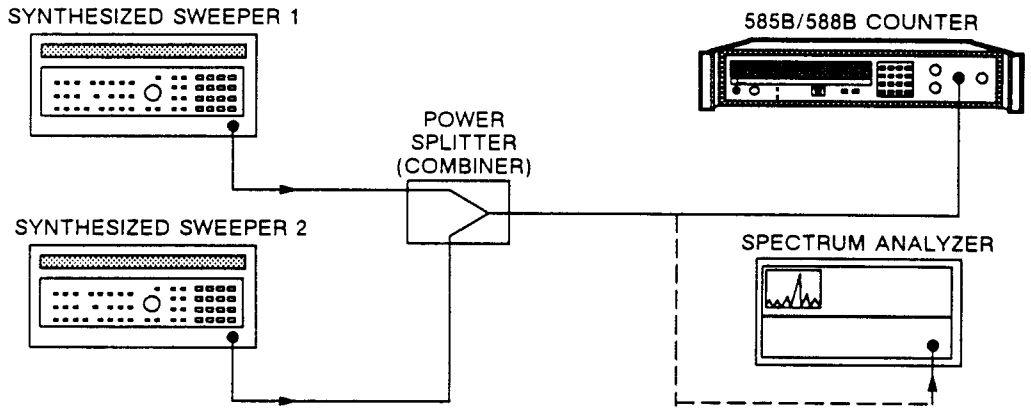

Figure 8-7. Band 2 Amplitude Discrimination Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-7.
2. Set synthesized sweeper 1 to 3 GHz at 0 dBm and set synthesized sweeper 2 to 3.1 GHz at -15 dBm.
3. Verify that 585B/588B counter correctly measures the frequency of the high power signal source.
4. Repeat steps 2 and 3 at 6 GHz and 6.1 GHz, at 12 GHz and 12.1 GHz, and at 18 GHz and 18.1 GHz.

BAND 1 GATE ERROR TEST

Description

This test verifies that the gate error in Band 1 is within the limits defined by the equation:

$$GE = (\pm 0.07) \ / \ (GW)$$

where GE is the gate error in Hz
GW, in seconds, is the logical AND of inhibit and pulse width minus 30 ns

The measurement is performed with a CW input signal and an inhibit signal.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)

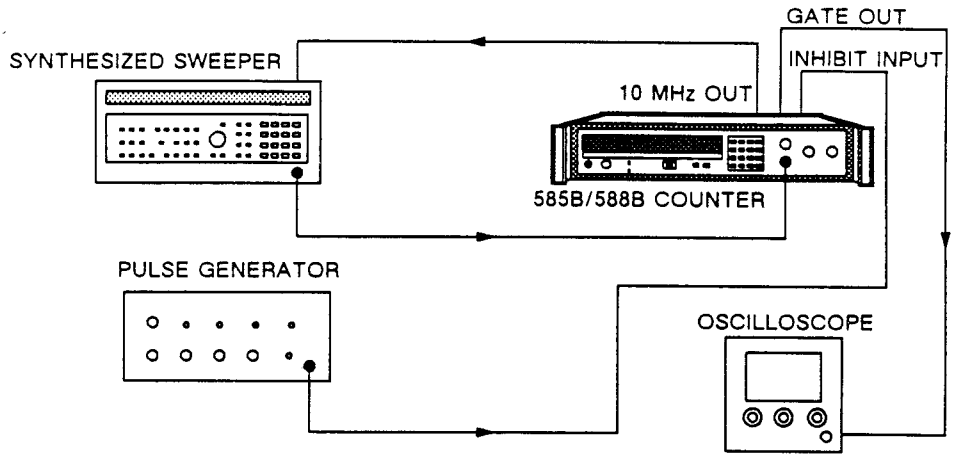

Figure 8-8. Band 1 Gate Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-8 and turn equipment on.

2. Set pulse generator to complementary mode, 0 to -1 volt pulse amplitude measured with 50 ohms load, 1 MHz PRF, and 50 ns pulse width.

3. Set 585B/588B counter to Band 1; set averaging feature to 99.

4. Set synthesized sweeper frequency to 300 MHz and power to 0 dBm. The CW reading on the counter display should be equal to the input frequency ±1 kHz.

5. Connect pulse generator output to inhibit input of counter. Connect gate output from counter to oscilloscope. Adjust inhibit pulse width until average gate width is 20 ns. Verify that reading on counter display is within limits of gate error.

6. Repeat step 4 and 5 with 100 ns and 1 μs gate width while keeping duty cycle (the ratio of pulse width to pulse period) constant.

7. Repeat measurements at 650 MHz and 1 GHz.

BAND 2 GATE ERROR TEST

Description

This test verifies that the gate error in Band 2 is within the limits defined by the equation:

$$GE = (\pm 0.01) \ / \ (GW)$$

where GE is the gate error in Hz
GW, in seconds, is the logical AND of inhibit and pulse width minus 30 ns

The measurement is performed with a CW input signal and an inhibit signal.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
Low attenuation coaxial cable (Gore P2S01S01036.0)

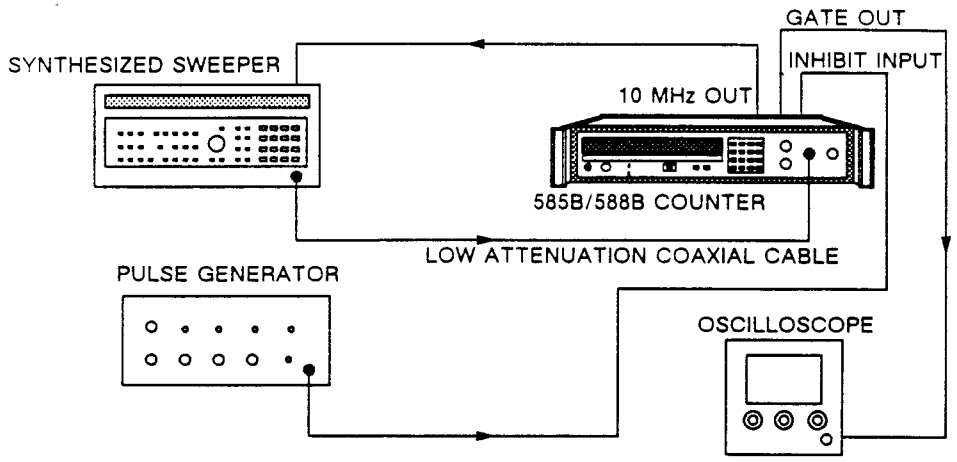

Figure 8-9. Band 2 Gate Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-9 and turn equipment on.
2. Set pulse generator to complementary mode, 0 to -1 volt pulse amplitude measured with 50 ohms load, 1 MHz PRF, and 50 ns pulse width.
3. Set 585B/588B counter to Band 2; set averaging feature to 99.
4. Set synthesized sweeper frequency to 3 GHz and power to 0 dB. The CW reading on counter display should be equal to input frequency ±1 kHz.
5. Connect pulse generator output to inhibit input of counter. Connect gate output from counter to oscilloscope. Adjust inhibit pulse width until average gate width is 20 ns. Verify that the reading on counter display is within limits of gate error.
6. Repeat step 4 and 5 with 100 ns and 1 μs gate width while keeping duty cycle (the ratio of pulse width to pulse period) constant.
7. Repeat measurements every 3 GHz up to 20 GHz (26.5 GHz for the 588B counter).

BAND 1 DISTORTION ERROR TEST

Description

This test verifies that the distortion error in Band 1 is within the limits defined by the equation:

$$DE = (+0.03) / (PW - 30\ ns)$$

where DE is distortion error in Hz
PW is pulse width in seconds

The measurement is performed by counting the frequency of a pulsed signal and subtracting the gate error from the result.

NOTE

Gate error must be known (see gate error test in this section) before performing this test.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse generator (Wavetek 801)
Pulse modulator (250 MHz to 1 GHz) (see "Special Equipment")
Oscilloscope (Tektronix 475)
6 dB attenuator (DC to 1 GHz) (Texscan FP-50)
Detector (Hewlett Packard 8473B)

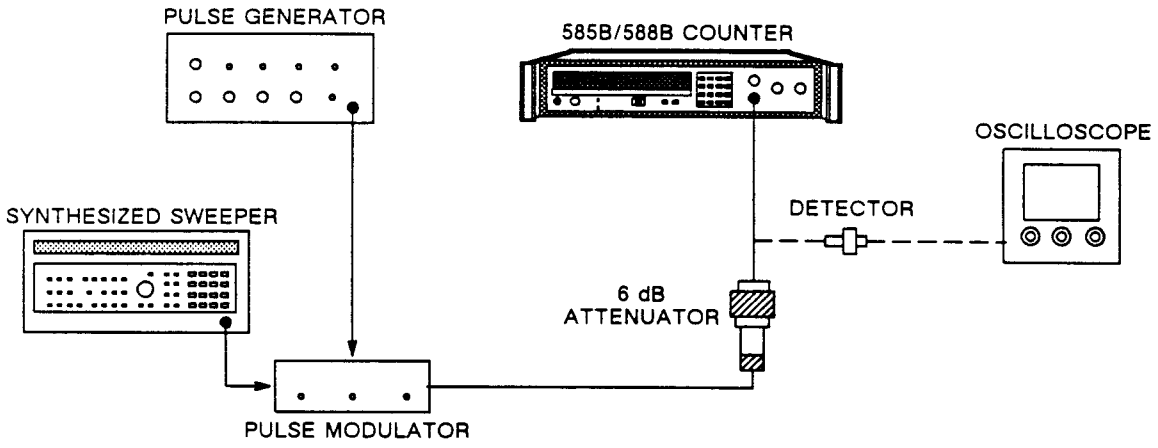

Figure 8-10. Band 1 Distortion Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-10. The 6 dB attenuator should be at the input of counter. Turn equipment on.
2. Set 585B/588B counter to Band 1; set average to 99.
3. Connect signal to oscilloscope as shown. Set synthesized sweeper frequency to 250 MHz and power to +10 dBm.
4. Set pulse generator to 1 MHz PRF, 50 ns pulse width, and +3.0 to -0.5 volts.
5. Adjust pulse width and voltage levels slightly until pulsed RF signal is 50 ns wide and has a good on/off ratio.
6. Take one measurement.
7. Calculate:

   Distortion Error = (Current Measurement) - (Gate Error)

   Gate error is error measured by gate error test in this section.

8. Verify that distortion error is within specification.

9. Repeat steps 4 to 8 with 100 ns and 1 μs pulse width while keeping duty cycle (the ratio of pulse width to pulse period) constant.

10. Repeat steps 4 to 9 every 100 MHz up to 1 GHz.

BAND 2 DISTORTION ERROR TEST

Description

This test verifies that the distortion error in Band 2 is within the limits defined by the equation:

$$DE = (\pm 0.03) / (PW - 3 \times 10^{-8})$$

where DE is distortion error in Hz
PW is pulse width in seconds

The measurement is performed by counting the frequency of a pulsed signal and subtracting the gate error from the result.

Equipment Required

Synthesized sweeper(Hewlett Packard 8340B)
Pulse modulator (Hewlett Packard 11720A)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
3 dB attenuators (3) (Weinschel 9-3)
Low attenuation coaxial cable (Gore P2S01S01036.0)
Detector (Hewlett Packard 8473B)

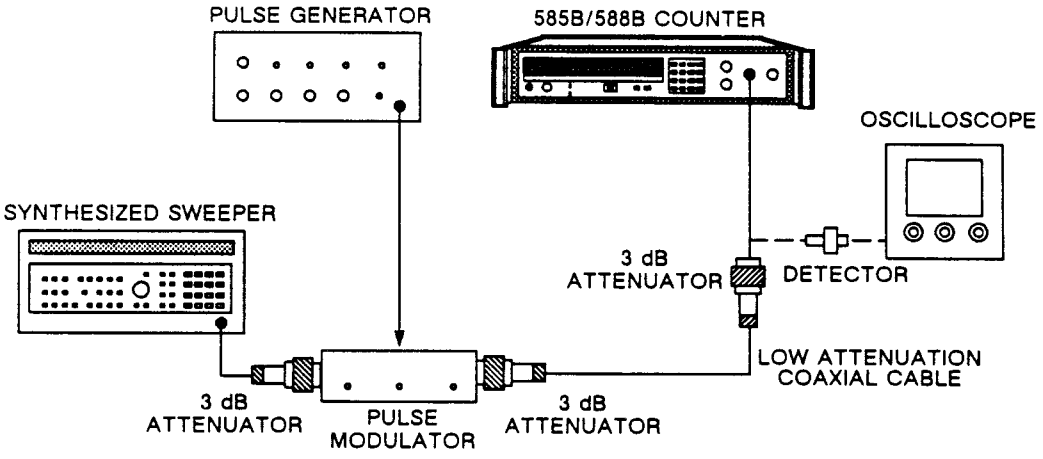

Figure 8-11. Band 2 Distortion Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-11. The 3 dB attenuators should be at IN and OUT ports of pulse modulator and at input to counter. Turn equipment on.

2. Set 585B/588B counter to Band 2; set averaging feature to 99.

3. Connect signal through detector to oscilloscope as shown. (Detector must be terminated in a low impedance device, such as a 50 ohm feedthrough, to detect narrow pulses adequately.) Set synthesized sweeper frequency to 2 GHz and power to +10 dBm.
4. Set pulse generator to 1 MHz PRF, 50 ns pulse width, and +3.0 to -0.5 volts.
5. Adjust pulse width and voltage levels slightly until pulsed RF signal is 50 ns wide and has a good on/off ratio.
6. Take one measurement.
7. Calculate:

   Distortion Error = (Current Measurement) - (Gate Error)

   Gate error is error measured by gate error test in this section.
8. Verify that distortion error is within specification.
9. Repeat steps 4 to 8 with 100 ns, and 1 μs, pulse width while keeping duty cycle (the ratio of pulse width to pulse period) constant.
10. Repeat steps 5 through 9 at 10 GHz and 18 GHz.

BAND 1 AVERAGING ERROR TEST

Description

This test verifies that the averaging error in Band 1 is within the limits defined by the equation:

$$AE = \pm(2)\sqrt{[RES\ /\ (GW)(AVG)]}$$

where AE is the RMS averaging error in Hz.

RES is the specified instrument resolution in Hz. (This is true up to 1 MHz resolution. Above 1 MHz resolution, RES is 1 MHz.)

GW, in seconds, is the logical AND of inhibit and pulse width minus.

3×10^{-8} seconds. For this test, gate width will be set to 20 ns.

AVG is the number of specified count average. The measurement is performed by counting the frequency of n pulsed signals and calculating the standard deviation given as:

$$S = \sqrt{\sum_{i=0}^{i=n-1} (F_i - F_{AVG})^2 / (n-1)} \quad \text{(standard deviation)}$$

where F_{AVG} is the average frequency measurement minus the gate error and the distortion error and F_i is the current reading.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)

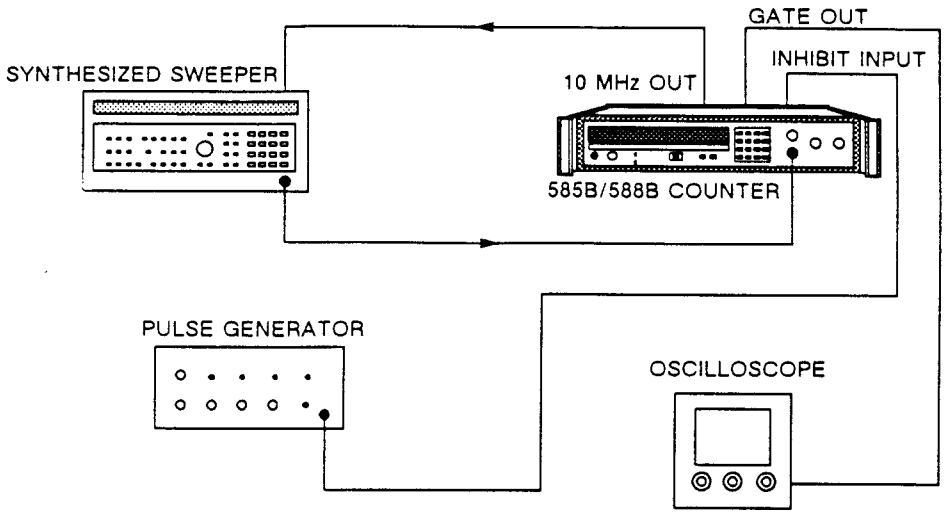

Figure 8-12. Band 1 Averaging Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-12 and turn equipment on.
2. Set pulse generator to complementary mode, 0 volt to -1 volt pulse amplitude measured with 50 ohms load, 1 MHz PRF, and 50 ns pulse width.
3. Set 585B/588B counter to Band 1; set averaging feature to 99.
4. Set synthesized sweeper frequency to 650 MHz and power to 0 dBm. CW reading on counter display should be equal to input frequency ±1 kHz.
5. Adjust inhibit pulse width until average gate width is 20 ns.
6. Take one frequency measurement. This reading is FAVG.
7. Turn averaging function off. Turn SAMPLE RATE knob on front panel to HOLD.
8. Take 10 measurements by pressing TRIG key 10 times.
9. Calculate:

$$S = \sqrt{\sum_{i=0}^{i=n-1} (F_i - F_{AVG})^2 / (n)}$$

10. Calculate:

$$AE = \pm(2)\sqrt{[RES / (GW)(AVG)]}$$

11. Verify that S < AE.

BAND 2 AVERAGING ERROR TEST

Description

This test verifies that the averaging jitter in Band 2 is within the limits defined by the equation:

$$AE = \pm\sqrt{[RES / (GW)(AVG)]}$$

where AE is the RMS averaging jitter in Hz.

RES is the specified instrument resolution in Hz. (This is true up to 1 MHz resolution. Above 1 MHz resolution, RES is 1 MHz.)

GW, in seconds, is the logical AND of inhibit and pulse width minus 3 x 10^{-8} seconds.

AVG is the number of specified count average.

The measurement is performed by counting the frequency of n pulsed signals and calculating the standard deviation given as:

$$S = \sqrt{\sum_{i=0}^{i=n-1} (F_i - F_{AVG})^2 / (n-1)} \qquad \text{(standard deviation)}$$

where FAVG is the average frequency measurement minus the gate error and the distortion error and Fi is the current reading.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
Low attenuation coaxial cable (Gore P2S01S01036.0)

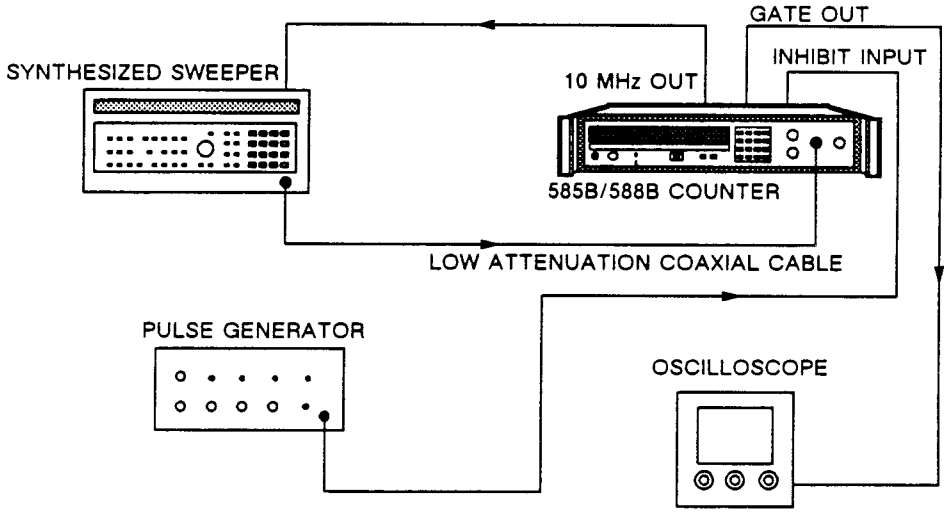

Figure 8-13. Band 2 Averaging Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-13 and turn equipment on.
2. Set pulse generator to complementary mode, 0 volt to -1 volt pulse amplitude measured with 50 ohm load, 1 MHz PRF, and 50 ns pulse width.
3. Set 585B/588B counter to Band 2; set averaging feature to 99.
4. Set synthesized sweeper frequency to 3 GHz and power to 0 dBm. CW reading on counter display should be equal to input frequency ±1 kHz.
5. Adjust inhibit pulse width until average gate width is 20 ns.
6. Take one frequency measurement. This reading is FAVG.
7. Turn averaging function off. Turn SAMPLE RATE knob to HOLD.
8. Take 10 measurements by pushing TRIG function key 10 times.
9. Calculate:

$$S = \sqrt{\sum_{i=0}^{i=n-1} (F_i - F_{AVG})^2 / (n-1)}$$

10. Calculate:

$$AE = \pm\sqrt{[RES / (GW)(AVG)]}$$

11. Verify that S < AE.

BAND 2 FREQUENCY LIMITS TEST

Description

This test verifies that the instrument will ignore signals outside of frequency limits.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Low attenuation coaxial cable (Gore P2S01S01036.0)

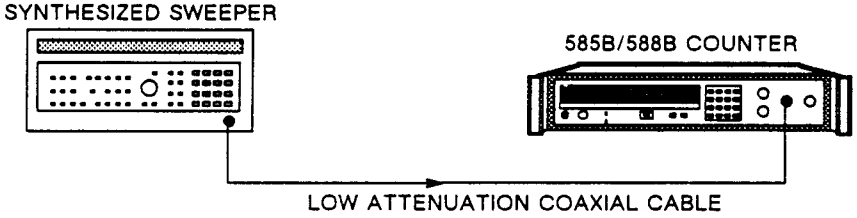

Figure 8-14. Band 2 Frequency Limits Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-14 and turn equipment on.
2. Set 585B/588B counter to Band 2 and press keys for FREQ LIMIT LOW, 3 GHz.
3. Set sweeper to low frequency limit minus 150 MHz and set power level to +7 dBm.
4. Increase sweeper frequency until frequency reading appears on display. Verify that this frequency is between low frequency limit minus 100 MHz and low frequency limit plus 50 MHz.
5. Clear frequency limit low. Press keys for FREQ LIMIT HIGH, 3 GHz.
6. Set sweeper to high frequency limit plus 150 MHz.
7. Decrease signal generator frequency until a frequency reading appears on display. Verify that this frequency is between high frequency limit plus 100 MHz and high frequency limit minus 50 MHz.

BAND 2 CENTER FREQUENCY TEST

Description

This test verifies that the counter locks on a signal +50 MHz from the center frequency.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Low attenuation coaxial cable (Gore P2S01S01036.0)

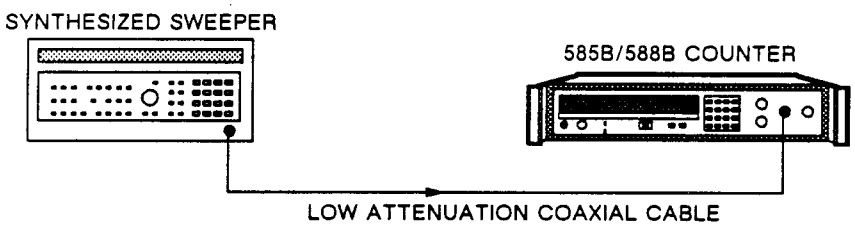

Figure 8-15. Band 2 Center Frequency Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-15 and turn equipment on.
2. Set 585B/588B counter to Band 2 and press keys for CENTER FREQUENCY 3 GHz.
3. Set sweeper to center frequency minus 50 MHz. Set power level to sensitivity level. Verify that reading on counter display is accurate.
4. Set sweeper to center frequency plus 50 MHz. Verify that reading on counter display is accurate.

BAND 1 MAXIMUM VIDEO

Description

This test verifies that frequency measurement accuracy is maintained in the presence of a video signal in excess of 20 dB below the RF signal.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Bidirectional coupler (Narda 3022)
Pulse generators (2) (Wavetek 801)
6 dB attenuator (Texscan FP-50)

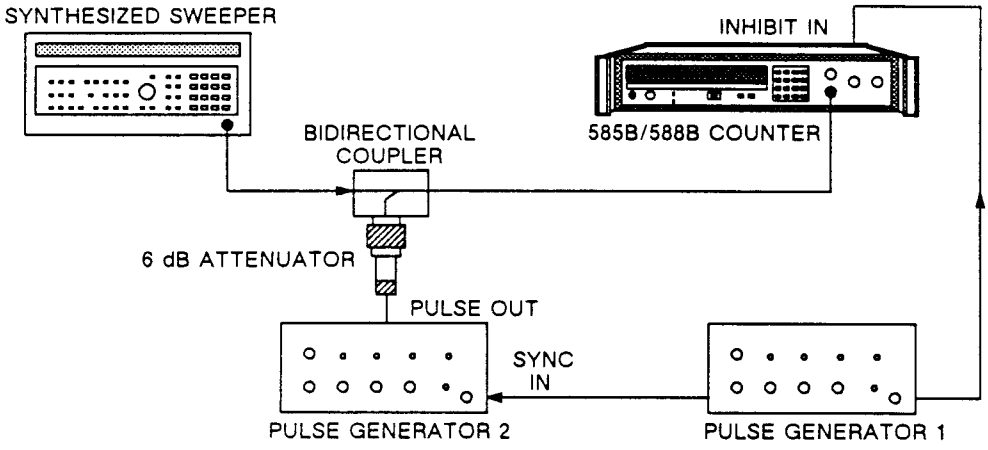

Figure 8-16. Band 1 Maximum Video Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-16 and turn equipment on.

2. Set pulse generator 1 to complementary mode, 0 to -1 volt pulse amplitude measured with a 50 ohm load, 1 MHz PRF, and 50 ns pulse width. This signal will be applied to INHIBIT IN connector on rear panel of counter.

3. Synchronize pulse generator 2 to pulse generator 1. Set pulse amplitude at 0 to 1 volt. Set time delay and pulse width so that pulses of both pulse generators overlap. Disable output of pulse generator 2. This signal will be applied to coupled port of bidirectional coupler.

4. Set 585B/588B counter to Band 1; set averaging feature to 99 pulses.

5. Set sweeper frequency to 300 MHz and power to +10 dBm at input to Band 1. Since CW signal is inhibited, reading on counter display includes some gate error.

6. Enable pulse generator 2. Verify that there is no change (besides that caused by averaging error) in the frequency reading.

7. Reverse polarity of both pulse generators and repeat step 6.

BAND 2 MAXIMUM VIDEO

Description

This test verifies that frequency measurement accuracy is maintained in the presence of a video signal in excess of 20 dB below the RF signal.

Equipment Required

Synthesized sweeper (HP 8340B)
Bidirectional coupler (Narda 3022)
Pulse generators (2) (Wavetek 801)
6 dB attenuator (Texscan FP-80)
Low attenuation coaxial cable (Gore P2S01S01036.0)

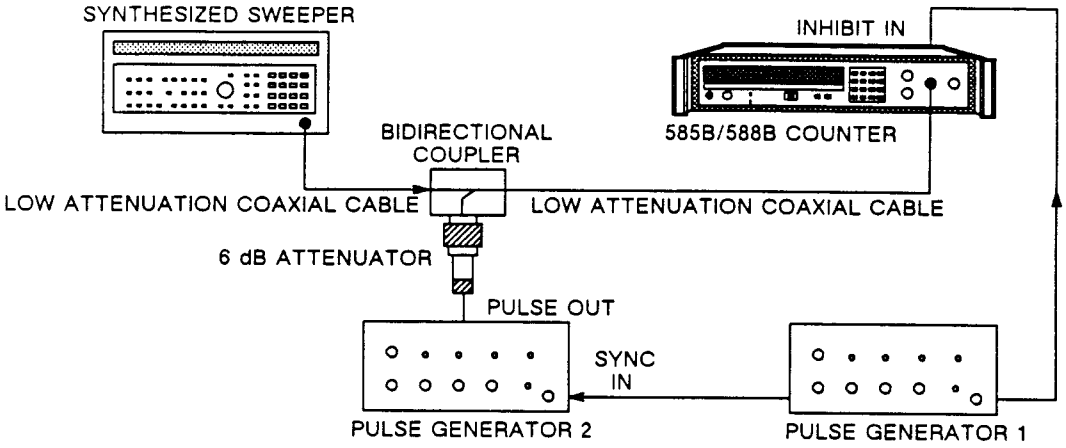

Figure 8-17. Band 2 Maximum Video Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-17 and turn equipment on.

2. Set pulse generator 1 to complementary mode, 0 to -1 volt pulse amplitude measured with a 50 ohm load, 1 MHz PRF, and 50 ns pulse width. This signal will be applied to INHIBIT IN connector on rear panel of counter.

3. Synchronize pulse generator 2 to pulse generator 1. Set pulse amplitude at 0 to 1 volt. Set time delay and pulse width so that pulses of both pulse generators overlap. Disable output of pulse generator 2. This signal will be applied to coupled port of bidirectional coupler.

4. Set 585B/588B counter to Band 2; set averaging feature to 99 pulses.

5. Set sweeper frequency to 3 GHz and power to +10 dBm at input to Band 2. Since CW signal is inhibited, reading on counter display includes some gate error.

6. Enable pulse generator 2. Verify that there is no change (besides that caused by jittering error) in the frequency reading.

7. Reverse polarity of both pulse generators and repeat step 6.

PULSE WIDTH ACCURACY TEST

This test verifies that the pulse width accuracy is within ±20 ns.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse modulator (Hewlett Packard 11720A)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
3 dB attenuator (up to 26.5 GHz) (3) (Weinschel 9-3)
Low attenuation coaxial cable (Gore P2S01S01036.0)
Detector (Hewlett Packard 8473B)

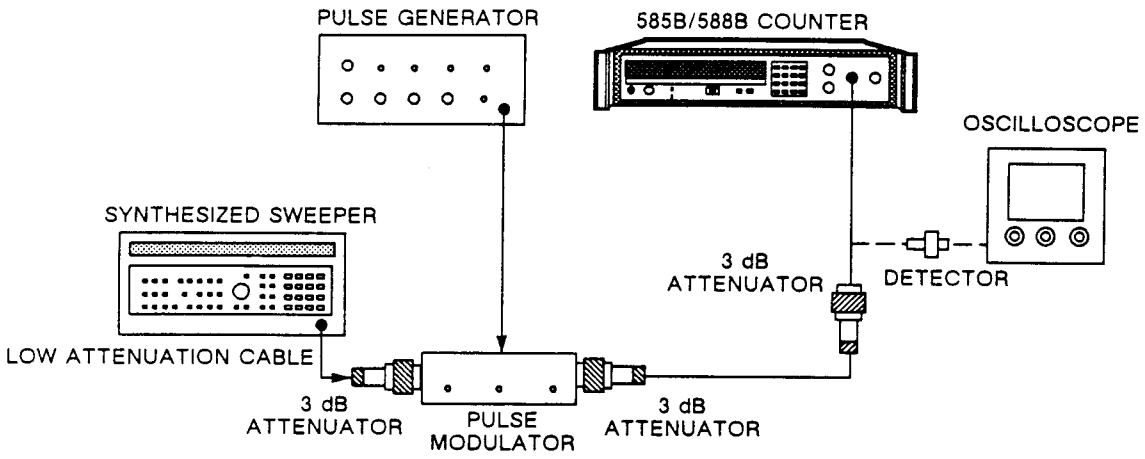

Figure 8-18. Pulse Width Accuracy Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-18. The 3 dB attenuators should be at IN and OUT ports of pulse modulator and input to counter. Turn equipment on.

2. Set 585B/588B counter to Band 2; set averaging feature to 99.

3. Connect signal through detector to oscilloscope as shown. Detector must be terminated in a low impedance device such as a 50 ohm feedthrough, to detect narrow pulses adequately. Set sweeper frequency to 2 GHz and power to +10 dBm.

4. Set pulse generator to 1 MHz PRF, 50 ns pulse width, and +3.0 to -0.5 volts.

5. Connect signal to counter and turn pulse width on. Verify that pulse width is 0.05 µs ±0.02 µs.

PULSE PERIOD ACCURACY TEST

This test verifies that the pulse period accuracy is within ±20 ns.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Pulse modulator (Hewlett Packard 11720A)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
3 dB attenuators (up to 26.5 GHz) (3) (Weinschel 9-3)
Low attenuation coaxial cable (Gore P2S01S01036.0)
Detector (Hewlett Packard 8473B)

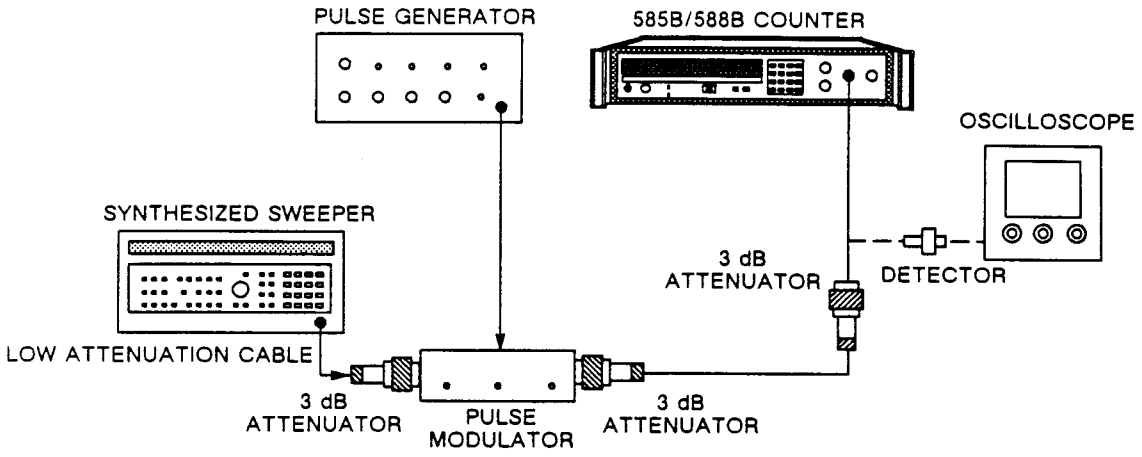

Figure 8-19. Pulse Period Accuracy Test Setup.

Procedure

1. Connect equipment as shown in Figure 8-19. The 3 dB attenuators should be at IN and OUT ports of pulse modulator, and input to counter. Turn equipment on.

2. Set 585B/588B counter to Band 2; set averaging feature to 99.

3. Connect signal through detector to oscilloscope as shown. Detector must be terminated in a low impedance device, such as a 50 ohm feedthrough, to detect narrow pulses adequately. Set sweeper frequency to 2 GHz and power to +10 dBm.

4. Set pulse generator to 1 MHz PRF, 50 ns pulse width, and +3.0 to -0.5 volts.

5. Connect signal to counter and turn pulse period on. Verify that pulse period is 1 μs ±0.02 μs.

SECTION 9
TROUBLESHOOTING

INTRODUCTION

This section defines troubleshooting aids that can be used to identify malfunctions within the 585B/588B counters. They are:

1. Signature analysis
2. Self diagnostics
3. Keyboard-controlled circuit tests
4. Troubleshooting trees

The procedures and tables provided in this section are for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a four-character alphanumeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information generates a signature unique to that data string. That signature can then be compared to a reference signature taken from a known good product to determine if the data string is correct. The counter implements signature analysis in either a free-running or program-controlled manner.

When performing signature analysis, the processor board is set up in a free-running mode by removing the header in A5E1 and grounding E1 pin 9 and E1 pin 11. This forces an internal CPU instruction onto the bus, such as NOP. In turn, this causes the processor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections from the signature analyzer, the user can probe the entire bus system for bad signatures. Processor free-running signatures are listed in Table 9-1.

Table 9-1. Processor Free-Running Signatures.

	Start	Stop	Clock
Connections	A5 TP3	A5 TP3	A5 TP4
Buttons	In	In	In

NOTE

The signatures shown below are taken using the HP 5004A Signature Analyzer.

Line	Signature
A0 (P1 Pin 54)	UUUU
A1 (P1 Pin 53)	FFFF
A2 (P1 Pin 52)	8484
A3 (P1 Pin 51)	P763
A4 (P1 Pin 50)	1U5P
A5 (P1 Pin 49)	0356
A6 (P1 Pin 48)	U759
A7 (P1 Pin 47)	6F9A
A8 (P1 Pin 46)	7791
A9 (P1 Pin 45)	6321
A10 (P1 Pin 44)	37C5
A11 (P1 Pin 43)	6U28
A12 (P1 Pin 42)	4FCA
A13 (P1 Pin 41)	4868
A14 (P1 Pin 40)	9UP1
A15 (P1 Pin 39)	0001
I/O (P1 Pin 11)	U3P4
U5 Pin 13	9F14
U5 Pin 16	4H16
U5 Pin 17	U3P7
U5 Pin 18	854F
U5 Pin 19	PACF

SELF-DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests, it then enters the normal operating mode. If the counter fails any checks, an error number is displayed. Refer to error message listing at the end of Section 3 to determine cause of error.

KEYBOARD-CONTROLLED CIRCUIT TESTS

There are seven keyboard-controlled circuit tests (01 through 07). All tests are accessed by pressing SPECIAL FUNC and the two-digit test number. Tests that do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07) can be exited by pressing any key. This causes the counter to exit the test and enter the functions selected. Test 05, which uses the keyboard in its operation, can be exited by pressing CLEAR DISPLAY. This causes the counter to return to normal operation.

01 **100 MHz Self Test.** This test sets the VCO to 400 MHz, divides it by four, and counts the 100 MHz output from the divider. It checks the count chain, VCO, VCO phase lock circuitry, and the gate generator.

02 **Display 8s Test.** This test lights all LEDs, annunciators, and decimal points. It checks that everything on the display is operational.

03 **Display Segment Test.** This test lights each segment of each digit and each annunciator one at a time, cycling through all segments. The cycle rate can be adjusted using the SAMPLE RATE control. It verifies that each segment of the display, segment drivers, and display multiplexer operate properly and independently.

04 **Display Digit Test.** This test lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the settings of the SAMPLE RATE control. It checks each digit and digit driver independently and verifies operation of the display multiplexer.

05 **Keyboard Test.** This test displays the key code of each key as it is pressed. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The key codes (coordinates) for each key are shown in Table 9-3.

Table 9-2. Keyboard Test Coordinates.

Key	Key Code
7	11
8	12
9	13
GHz	14
4	21
5	22
6	23
MHz	24
1	31
2	32
3	33
kHz	34
±	41
0	42
.	43
Hz	44
PULSE WIDTH	51
PULSE PERIOD	52
CLEAR DATA	53
INIT/LOCAL	61
CLEAR DISPLAY	EXIT TEST

06 **PROM Check Sum Test.** This test generates the check sum for the PROM in the counter and compares it with the check sum stored in the firmware. If the check sum generated is correct, the counter displays the word "PASSEd". If the check sum is incorrect, an Error 61 message is output to the display.

07 **Display Counter Model Number.** This function shows the user whether the counter is configured as a 585B or a 588B.

TROUBLESHOOTING TREES

The following troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any PC boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A1A1 Counter Interconnect
- A2 Power Supply
- A5 Processor
- A6 Count Chain
- A7 Gate Generator
- A8 Gate Control
- A9 Signal Conditioner

CAUTION

Do not attempt to repair or disassemble the A10 hybrid assembly.

TEST EQUIPMENT REQUIRED

Table 9-3. Troubleshooting Test Equipment.

Equipment	Range	Recommended Manufacturer	Model
Synthesized sweeper (2)	10 MHz to 26.5 GHz	Hewlett Packard	8340B
Frequency synthesizer	100 Hz to 10 MHz	Hewlett Packard	3325A
Sweep generator	3 to 18 GHz	Wiltron	6635B
Spectrum analyzer	100 Hz to 22 GHz	Hewlett Packard	8566B
Power meter	10 MHz to 60 GHz	Hewlett Packard	437B
Power sensor	10 MHz to 18 GHz	Hewlett Packard	8481A
Power sensor	50 MHz to 26.5 GHz	Hewlett Packard	8485A
Oscilloscope	DC to 100 MHz	Tektronix	475
Oscilloscope voltage probe	DC to 3.5 GHz	Tektronix	P6056
Power splitter	10 MHz to 26.5 GHz	Hewlett Packard	11667B
Directional coupler	10 to 1000 MHz	Anzac	CH132
Directional coupler	950 MHz to 18 GHz	Narda	4222-16
Directional coupler	18 to 26.5 GHz	Narda	4017C-10
Bidirectional coupler	10 dB	Narda	3022
Pulse generator (2)	5 Hz to 50 MHz	Wavetek	801
Pulse modulator	800 MHz to 2.4 GHz	Hewlett Packard	8731B
Pulse modulator	2 to 18 GHz	Hewlett Packard	11720A
Pulse modulator	18 to 26.5 GHz	Narda	S214DS
Low attenuation coaxial cable (3)		Gore	P2S01S01036.0
6 dB attenuator (2)	DC to 1 GHz	Texscan	FP-50
3 dB attenuator (3)	DC to 26.5 GHz	Weinschel	9-3
Detector	10 MHz to 18 GHz	Hewlett Packard	8473B
50 ohm termination		Pomona	4119-50

To use the troubleshooting trees.

1. Refer to the main troubleshooting tree.

2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.

3. Refer to the appropriate troubleshooting tree for that failure mode.

Before servicing any unit, verify that:

1. The line voltage and fuse are correct for the voltage setting.

2. Special Function 09 is selected (internal 10 MHz time base). If special function 08 is selected (external 10 MHz time base), check that a proper 10 MHz signal is applied to the 10 MHz IN/OUT connector.

3. The MIN PRF function is properly set. (See Section 3, Automatic Frequency Measurements.)

4. The counter is not inhibited by the rear panel inhibit input.

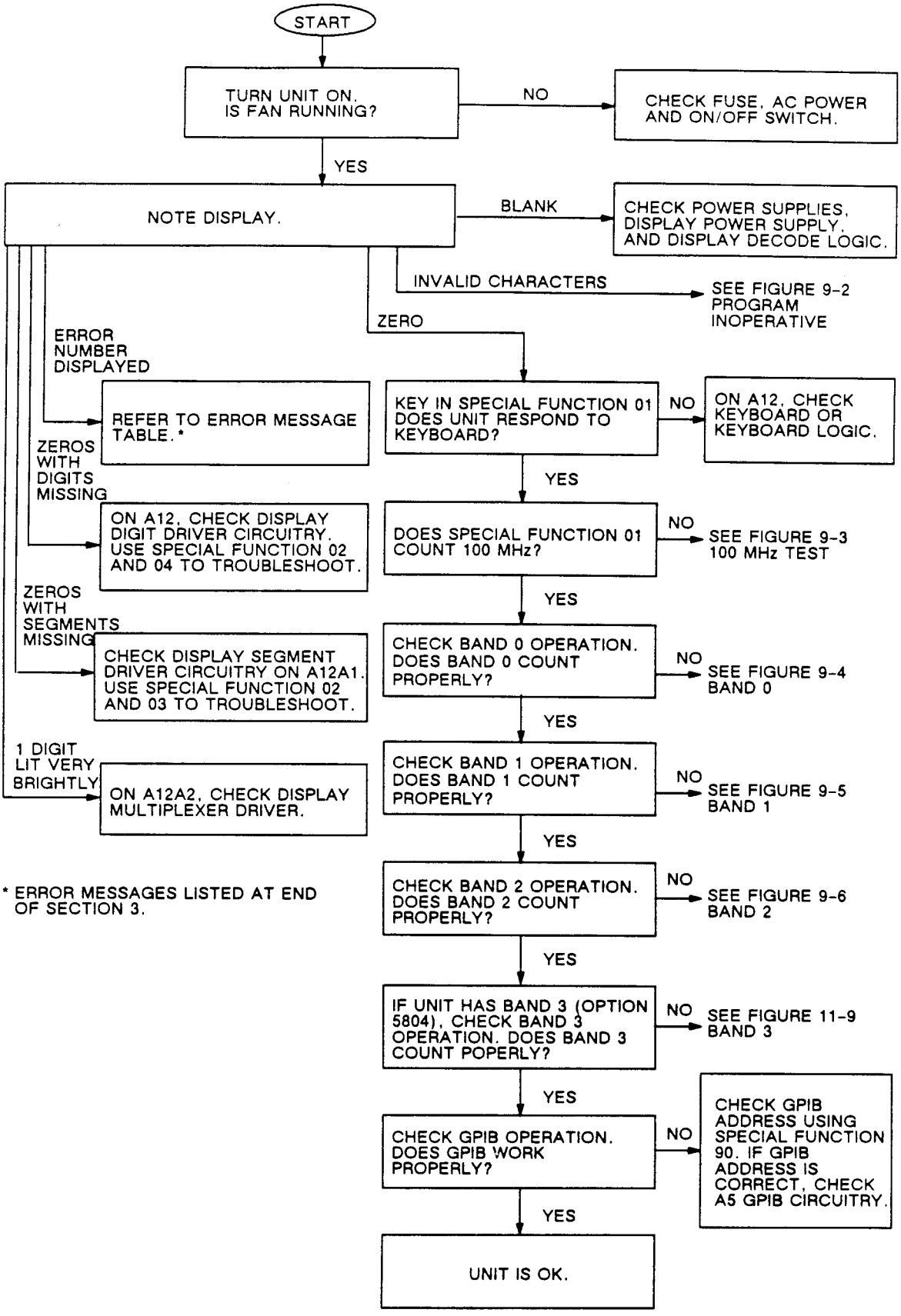

Figure 9-1. Main Troubleshooting Tree.

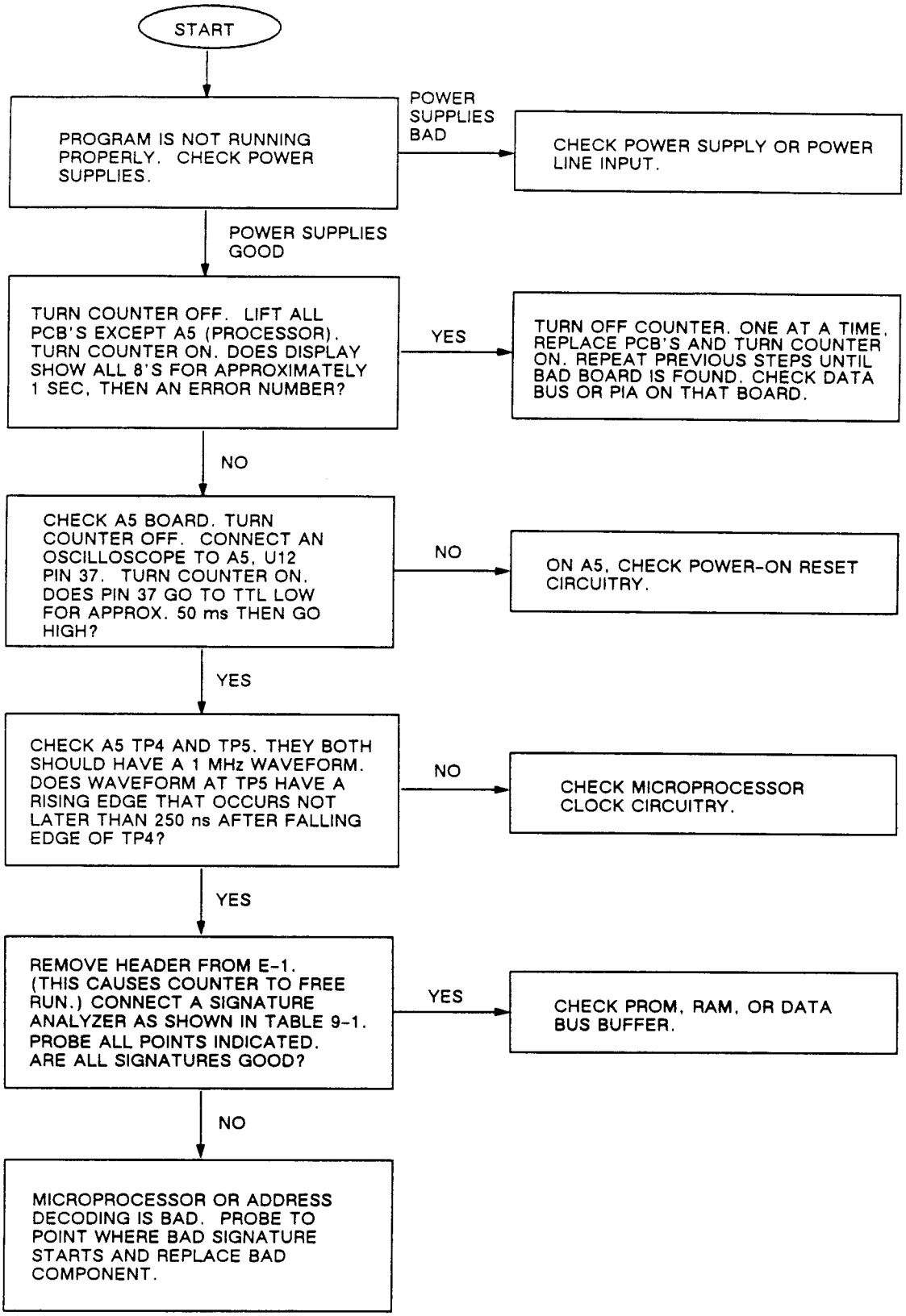

Figure 9-2. Program Inoperative Troubleshooting Tree.

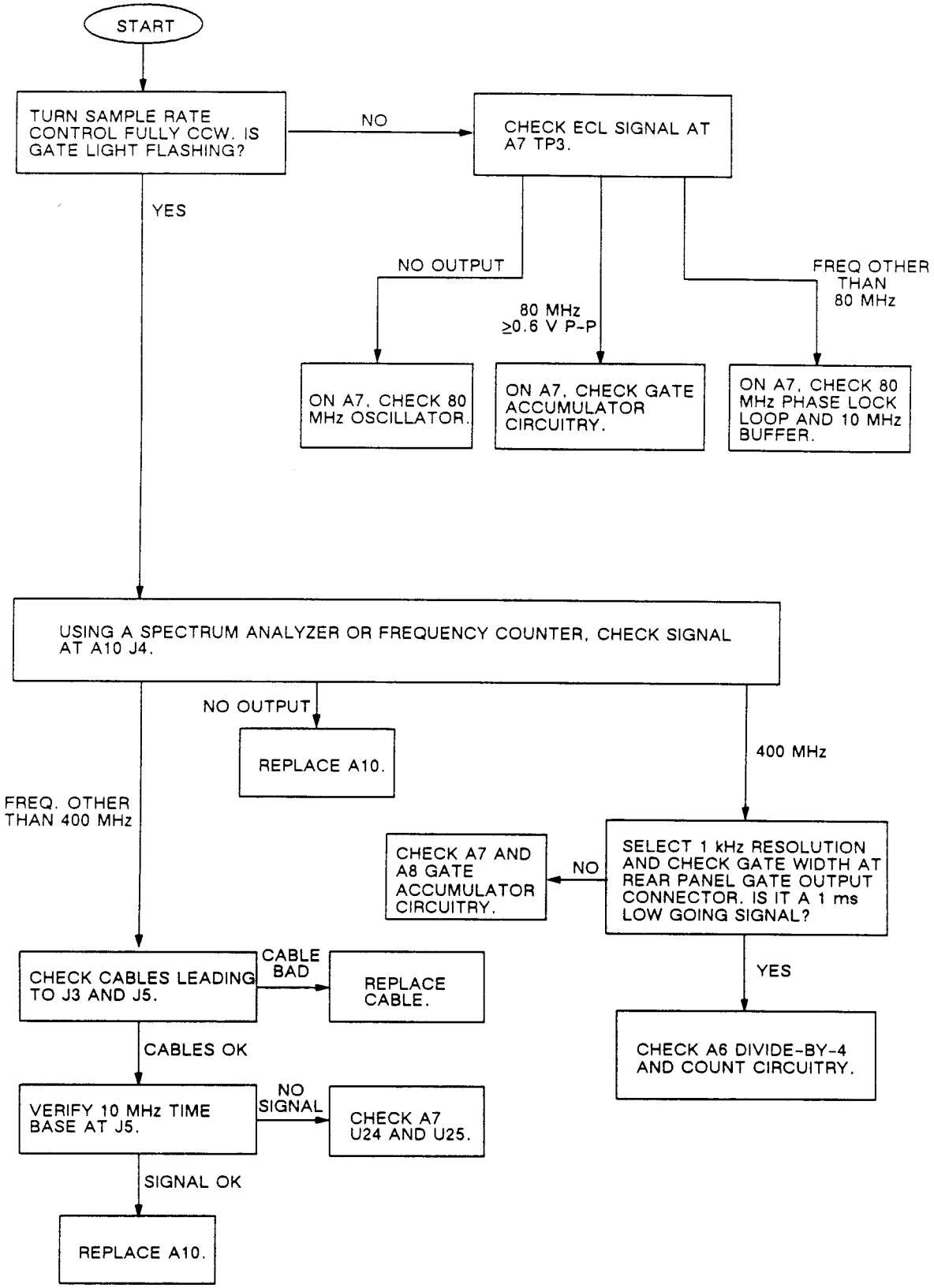

Figure 9-3. 100 MHz Self-test Troubleshooting Tree.

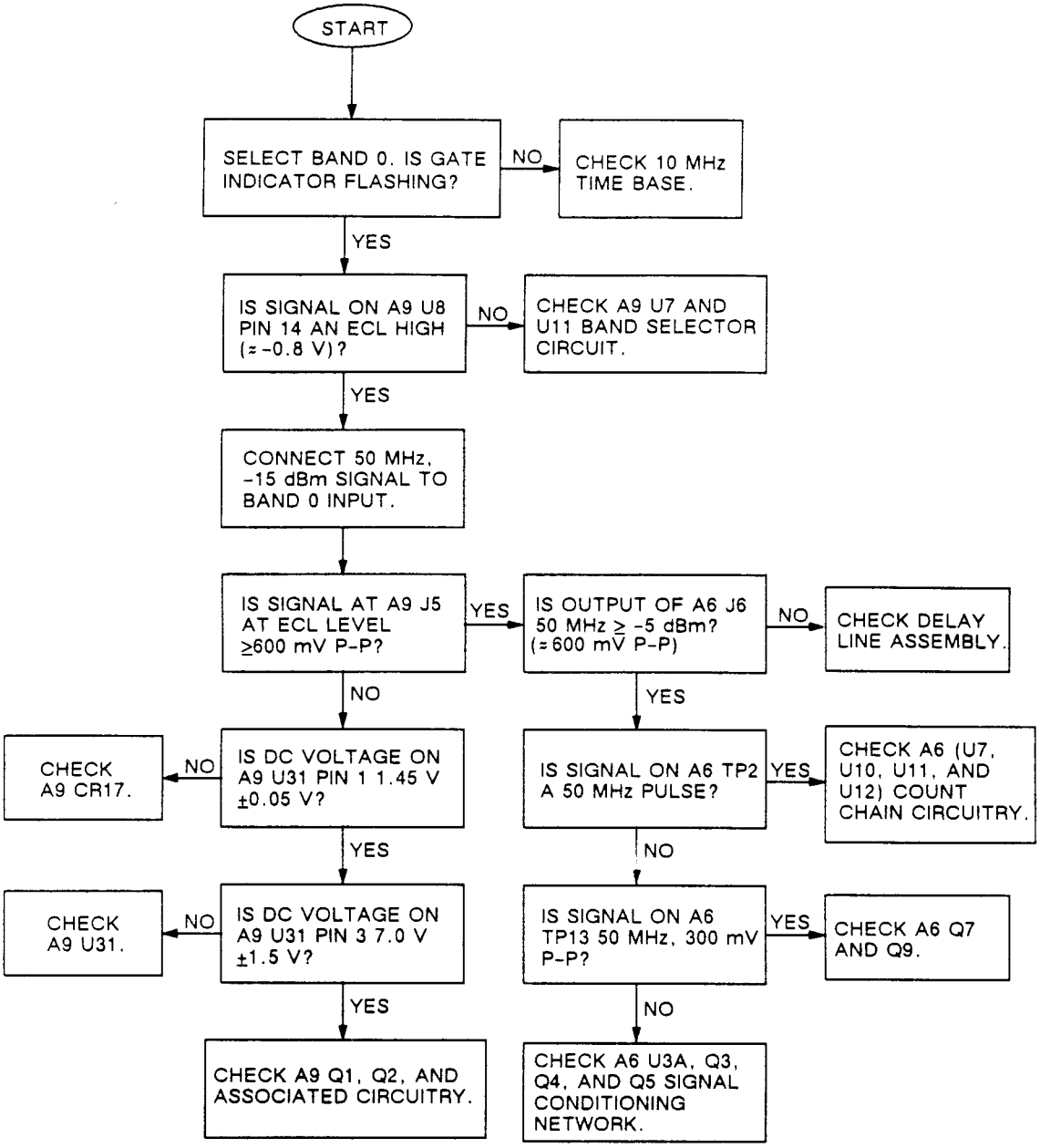

Figure 9-4. Band 0 Troubleshooting Tree.

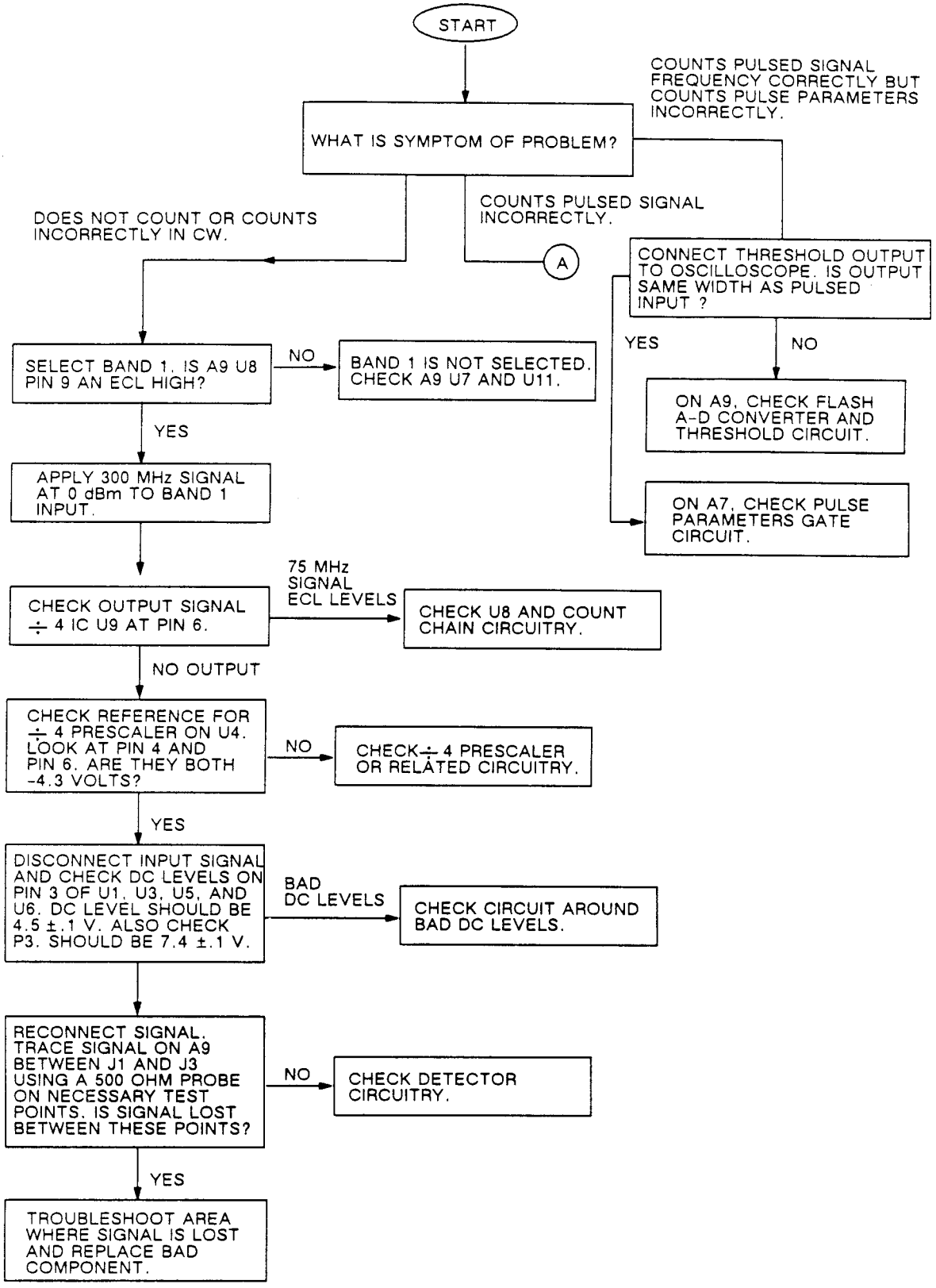

Figure 9-5. Band 1 Troubleshooting Tree.
(Sheet 1 of 2)

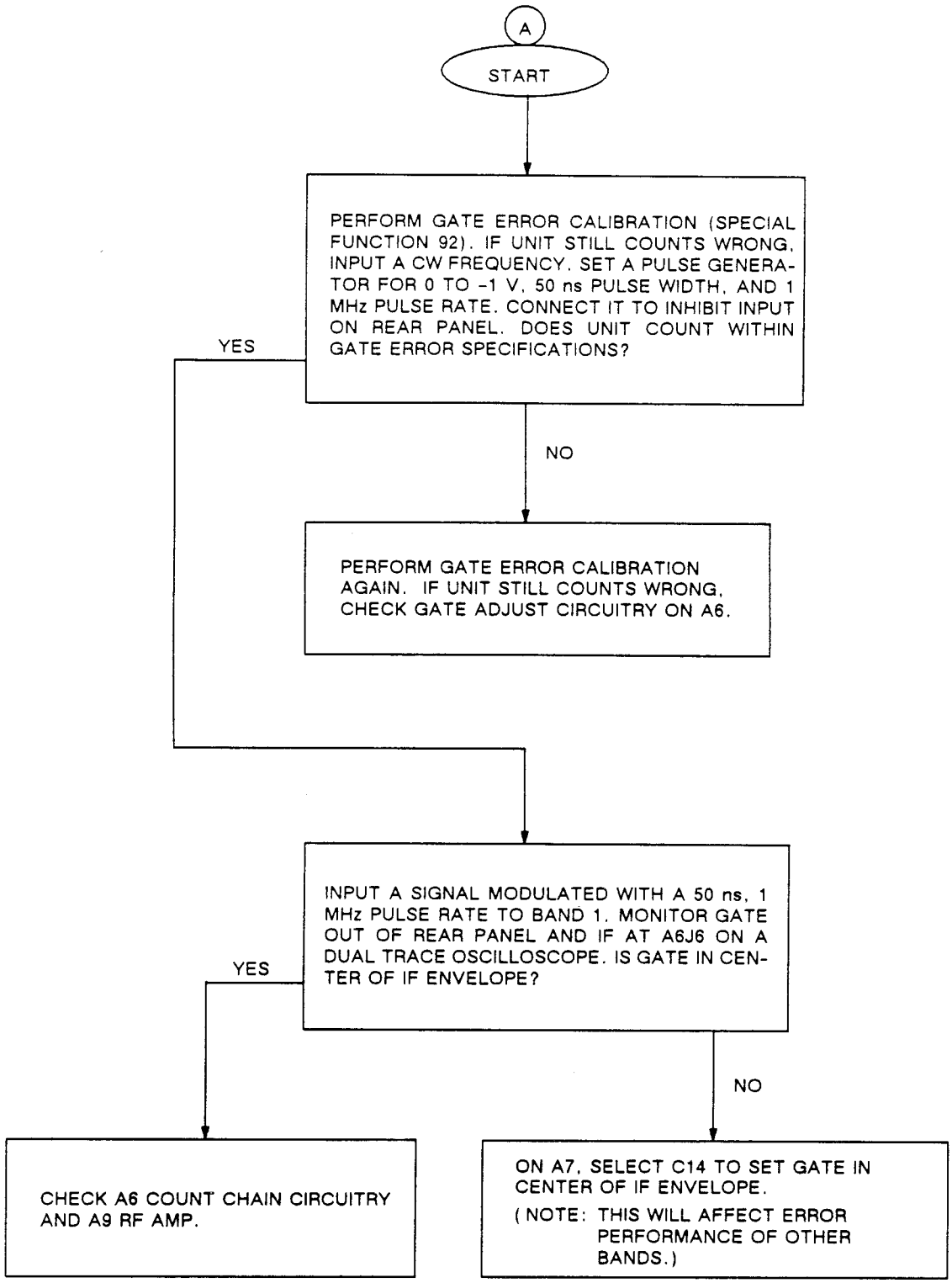

Figure 9-5. Band 1 Troubleshooting Tree.
(Sheet 2 of 2)

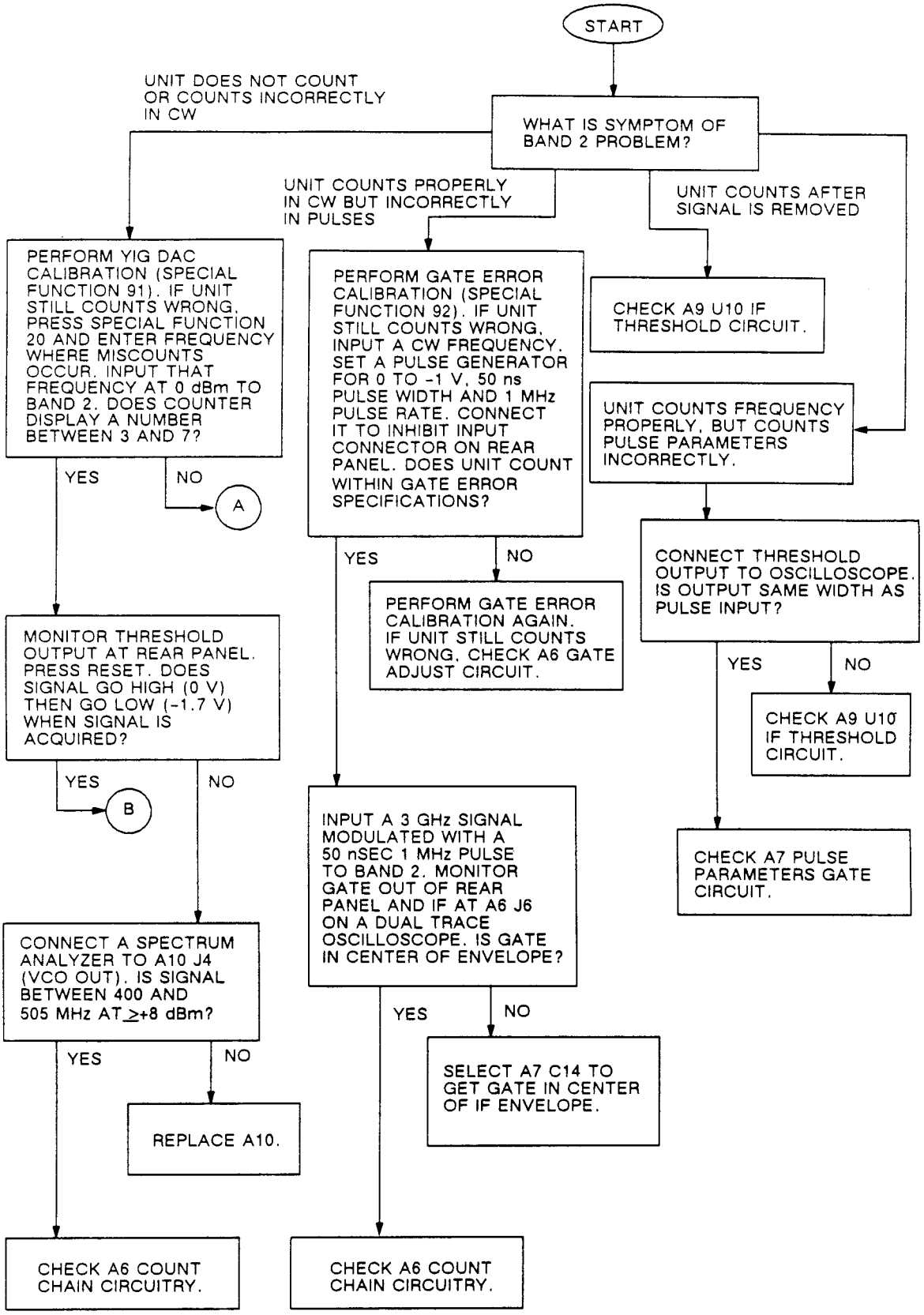

Figure 9-6. Band 2 Troubleshooting Tree.
(Sheet 1 of 2)

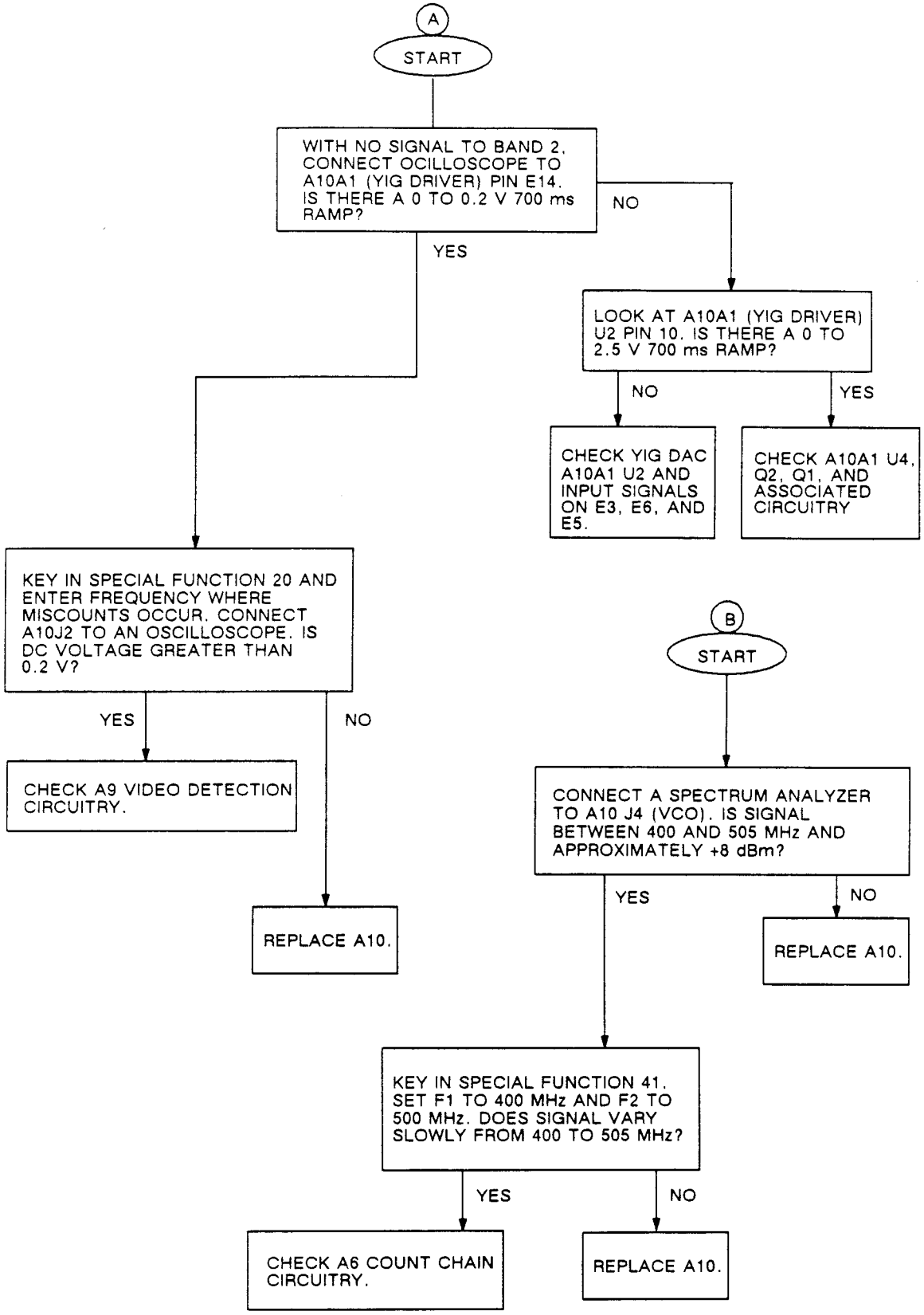

Figure 9-6. Band 2 Troubleshooting Tree. (Sheet 2 of 2)

SECTION 10
FUNCTIONAL DESCRIPTIONS AND REPLACEABLE PARTS

INTRODUCTION

This section contains functional descriptions, lists of replaceable parts, illustrations of component locations, and schematic diagrams for each assembly used in this counter.

The replaceable parts list for electrical assemblies (PCBs) lists the electrical components in alphanumerical order by reference designation. Components having different reference designators but having the same EIP part number are described for the first such component listed. Subsequent descriptions of that component refer to the first entry. The total number of like components used on the same assembly is listed with the first entry in the UNITS PER ASSY column.

The replaceable parts lists for mechanical assemblies is organized according to the item number sequence.

Similar functional descriptions and lists of replaceable parts for the available options are contained in Section 11, Options.

ORDERING INFORMATION

To order a replaceable part, quote the EIP part number, indicate the quantity required, and address the order to:

EIP Microwave, Inc.
Customer Support
1589 Centre Pointe Drive
Milpitas, CA 95035

To order a part that is not shown on the replaceable parts list, include the instrument model number, serial number, description and function of the part, and the number of parts required. Mail the order to the above address.

REFERENCE DESIGNATORS

A	Assembly	Q	Transistor
B	Battery or fan	R	Resistor
C	Capacitor	RN	Resistor network
CR	Diode	S	Switch
DS	Indicator (display)	T	Transformer
F	Fuse	TP	Test point
J	Jack	U	Integrated circuit
K	Relay	W	Wire or cable
L	Inductor	X	Socket or holder
P	Plug	Y	Crystal, piezoelectric

ABBREVIATIONS

A	ampere, assembly
A/D	analog-to-digital (converter)
AMP	amplifier
ASSY	assembly
ATTEN	attenuator
BCD	binary coded decimal
BLK	black
CAP	capacitor
CC	carbon composition
CER	ceramic
CMOS	complimentary metal oxide semiconductor
CNTR	counter
COAX	coaxial
CONN	connector
CONV	converter
COR	corner
CRES	corrosive resistant steel
CW	continuous wave
dB	deciBel
DAC	digital-to-analog converter
DEC	decade
DEG	degree
DET	detector
DIFF	differential
DIP	dual inline package
ECL	emitter-coupled logic
EEPROM	electrically erasable programmable memory
ELECTLT	electrolytic
EXCL	exclusive
FF	flip-flop
FR	front
FREQ	frequency
FRICTLK	friction lock
GHz	gigahertz (10^9 hertz)
GPIB	general purpose interface bus
GRN	green
GRY	gray
H	henry (inductance)
HARN	harness
HEX	hexadecimal, hexagon
HI SP	high speed
IC	integrated circuit
IF	intermediate frequency
INSUL	insulation
INTCON	interconnection
INTFC	interface
INTL	internal
I/O	input/output
k	kilo
kHz	kilohertz (10^3 hertz)
LED	light emitting diode
LO	local oscillator
LPF	low pass filter
LSB	least significant bit (byte)
LSD	least signicicant digit
MHz	megahertz (10^6 hertz)
MIN PRF	minimum PRF
µF	microfarad
MF	metallic film
µH	microhenry
µP	microprocessor
µs	microsecond
ML	mylar
MOD	model
MOM	momentary
M/OX	metal oxide
MS	monostable
MTG	mounting
MUX	multiplexer
NEG	negative
NPN	negative-positive-negative (transistor)
NPO	temperataure coefficient (capacitors)
NTWK	network
ns	nanosecond
OD	outside diameter
OCXO	oven controlled crystal oscillator
PAL	programmable array logic
PC	printed circuit
PCB	printed circuit board
pF	picofarad
PIA	peripheral interface adapter
PIN	positive intrinsic negative (diode)
PLL	phase locked loop
PNP	positive-negative-positive (transistor)
POT	potentiometer
prgm	program
PRF	pulse repetition frequency
PSVT	passivated
RAM	random access memory
RCPT	receptacle
RCVR	receiver
RECT	rectifier
REF	reference
REG	regulator (see also RGLTR)
res	resistor
RF	radio frequency
RGLTR	regulator (see also REG)
RN	resistor network
R/W	read/write
SB	slow blow (fuse)
SCR	screw
SEMS	screw/washer combination
SFLKG	self locking
SMD	surface mounted device
SPDT	single pole double throw
SQ	square
SRC	semirigid coax
SW	switch
TANT	tantalum
TCXO	temperature compensated crystal oscillator
TTL	transistor-transistor logic
UHF	ultrahigh frequency
UNC	unified coarse thread
UV	ultraviolet
VCO	voltage controlled oscillator
VAC	volts ac
VDC	volts dc
VHF	very high frequency
W	wire, watt
W/	with
W/MNT	with mount
W/O	without
XCVR	transciever
XFMR	transformer
X-REC	cross-reces (screw head)
XSTR	transistor
XTAL	crystal
X7R	temperature coefficient (capacitor)
YIG	ytrium-iron-garnet
YTF	YIG tune filter

TOP ASSEMBLY
2000068-04, -05 -06 (585B)
2000069-05, -06, -07, -08 (588B)

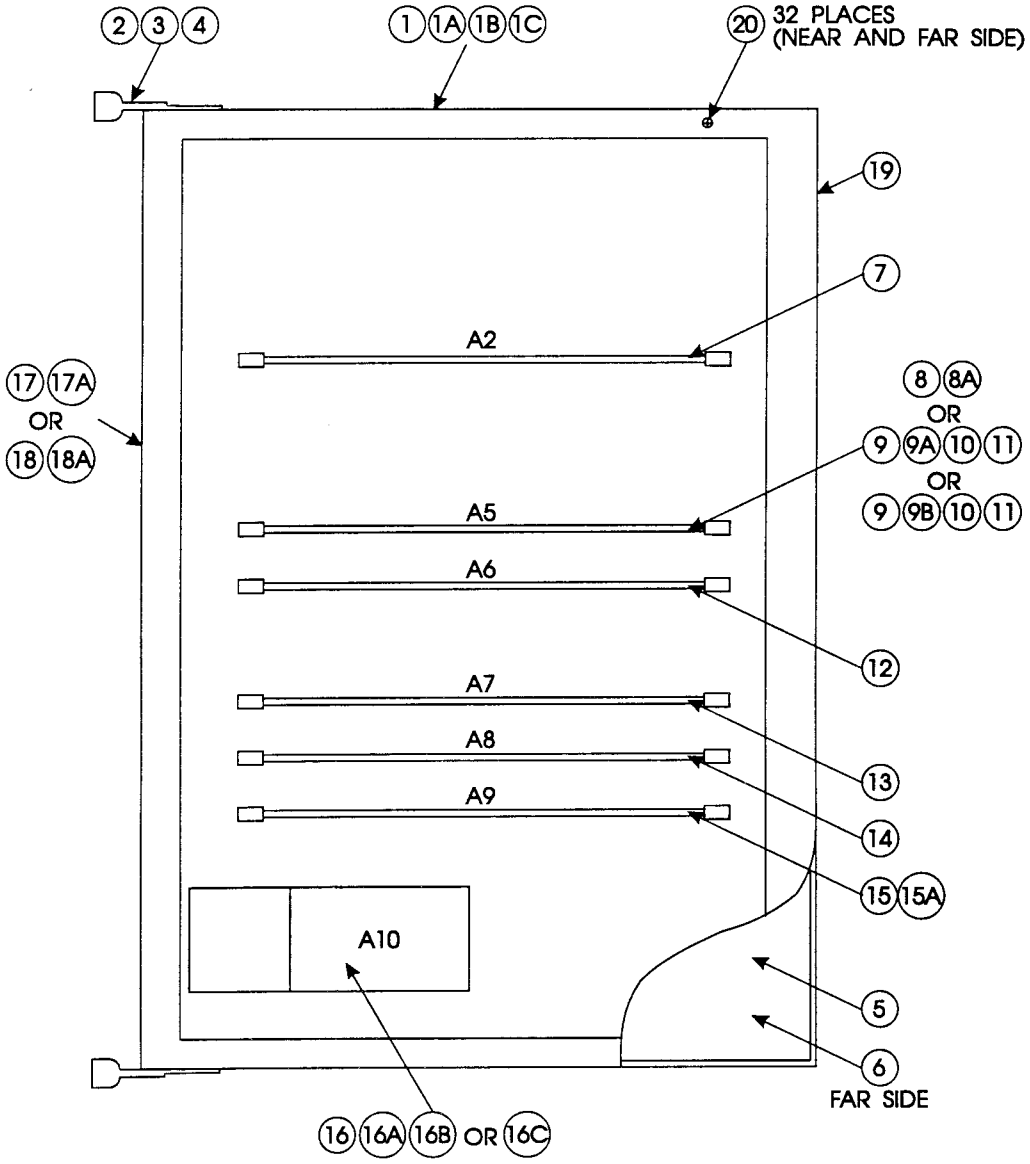

Figure 10-1. Top Assembly.

TOP ASSEMBLY

585B: CCN 6804/2000068-04
CCN 6805/2000068-05
CCN 6806/2000068-06

588B: CCN 6905/2000069-05
CCN 6906/2000069-06
CCN 6907/2000069-07
CCN 6908/2000069-08

ITEM NO.	DESCRIPTION	EIP NO.	UNITS PER ASSY
1	COUNTER ASSY,BASIC,585B **(CCN 6804)**	2010773-05	1
1A	COUNTER ASSY,BASIC,585B **(CCN 6805, 6806)**	2010773-06	1
1B	COUNTER ASSY,BASIC,588B **(CCN 6905, 6906)**	2010771-06	1
1C	COUNTER ASSY,BASIC,588B **(CCN 6907, 6908)**	2010771-07	1
2	HANDLE ASSY,REMOVABLE,BLK,3.50	2010402-02	2
3	NUT,FLANGE,8-32	5210441-01	2
4	SCR,FLH,X-REC,82D,8-32X5/16	5131008-05	2
5	COVER ASSY,TOP	2010765-01	1
6	COVER ASSY,BOTTOM	2010281-03	1
7	PCB ASSY,POWER SUPPLY	2020222-07	1
8	PCB ASSY,PROCESSOR **(585B: CCN 6804—588B: CCN 6905, 6906)**	2020400-02	1
8A	PROM,PRGM,PROCESSOR **(585B: CCN 6804—588B: CCN 6905, 6906)**	2060064-01	1
9	PCB ASSY,PROCESSOR **(585B: CCN 6805, 6806—588B: CCN 6907, 6908)**	2020480-02	1
9A	PROM,PRGM,PROCESSOR **(585B: CCN 6805, 6806—588B: CCN 6907, 6908)**	2060095-01	1
9B	PROM,PRGM,PROCESSOR **(585B: CCN 6806—588B: CCN 6908)**	2060106-01	1
10	PAL PRGMD,ADRS DEC **(585B: CCN 6805, 6806—588B: CCN 6907, 6908)**	2070099-01	1
11	CONN,JUMPER,2X6,.100 **(585B: CCN 6805, 6806—588B: CCN 6907, 6908)**	2620352-00	1
12	PCB ASSY,COUNT CHAIN	2020404-01	1
13	PCB ASSY,GATE GENERATOR	2020217-04	1
14	PCB ASSY,GATE CONTROL	2020405-02	1
15	PCB ASSY,SIGNAL CONDITIONER **(585B: CCN 6804—588B: CCN 6905)**	2020395-10	1
15A	PCB ASSY, SIGNAL CONDITIONER **(585B: CCN 6804, 6805, 6906) (588B: CCN 6905, 6906, 6907, 6908)**	2020395-12	1
16	CONVERTER ASSY,B2,585B **(CCN 6804)**	2010936-02	1
16B	CONVERTER ASSY,B2,585B **(CCN 6804, 6805, 6806)**	2010670-01	1
16A	CONVERTER ASSY,B2,588B **(CCN 6905)**	2010936-01	1
16C	CONVERTER ASSY,B2,588B **(CCN 6905, 6906, 6907, 6908)**	2010670-02	1
17	PANEL ASSY,FRONT,585B	2010803-03	1
17A	OVERLAY,FRONT PANEL,585B	5210842-01	1
18	PANEL ASSY,FRONT,588B	2010803-01	1
18A	OVERLAY,FRONT PANEL,588B	5210396-02	1
19	PANEL ASSY,REAR	2010763-02	1
20	SCR,FLH,X-REC 100DEG 6-32X5/16 UNC	5140006-05	32
	CORD,LINE 3-COND	5440002-00	1

Table 10-1. Cable Identification Guide.

From	Reference Designator	To	Description
Fan	W1	A2J2	Fan Power
Voltage select switch	W2	A1J11	Power Line Voltage Select (Option Power) *
A9J6	W3	A10J2	Video
A1T1	W4	A1J12	Power Line Voltage Select
Voltage select switch	W5	A1T1P1	Power Line Voltage Select
A6J1	W7	A10J3	VCO Out
A9J3	W8	A10J1	Band 2 IF
A1T1	W9	A12S1P1	Power Switch
A7J4	W10	A10J5	10 MHz
A10	W11	A1J5	Band 2 Power and Control
A12A2J6	W13	A1J1	Display Interface
A6P2	W14	A9J5	IF Delay Line
S1	W16	A1T1P3	Power Switch
A1T1	W17	A2J1/A101J1	Power
A9J1	A12W4	Front Panel	Band 0 Input
A9J8	A12W6	Front Panel	Band 1 Input
A1J2	A13W1	Rear Panel	GPIB Interface
A8J1	A13W2	Rear Panel	Inhibit Input
A8J2	A13W3	Rear Panel	Gate Output
A8J3	A13W4	Rear Panel	Signal Threshold Output
A7J3	A13W6	Rear Panel	10 MHz In/Out

* See Section 11, Options.

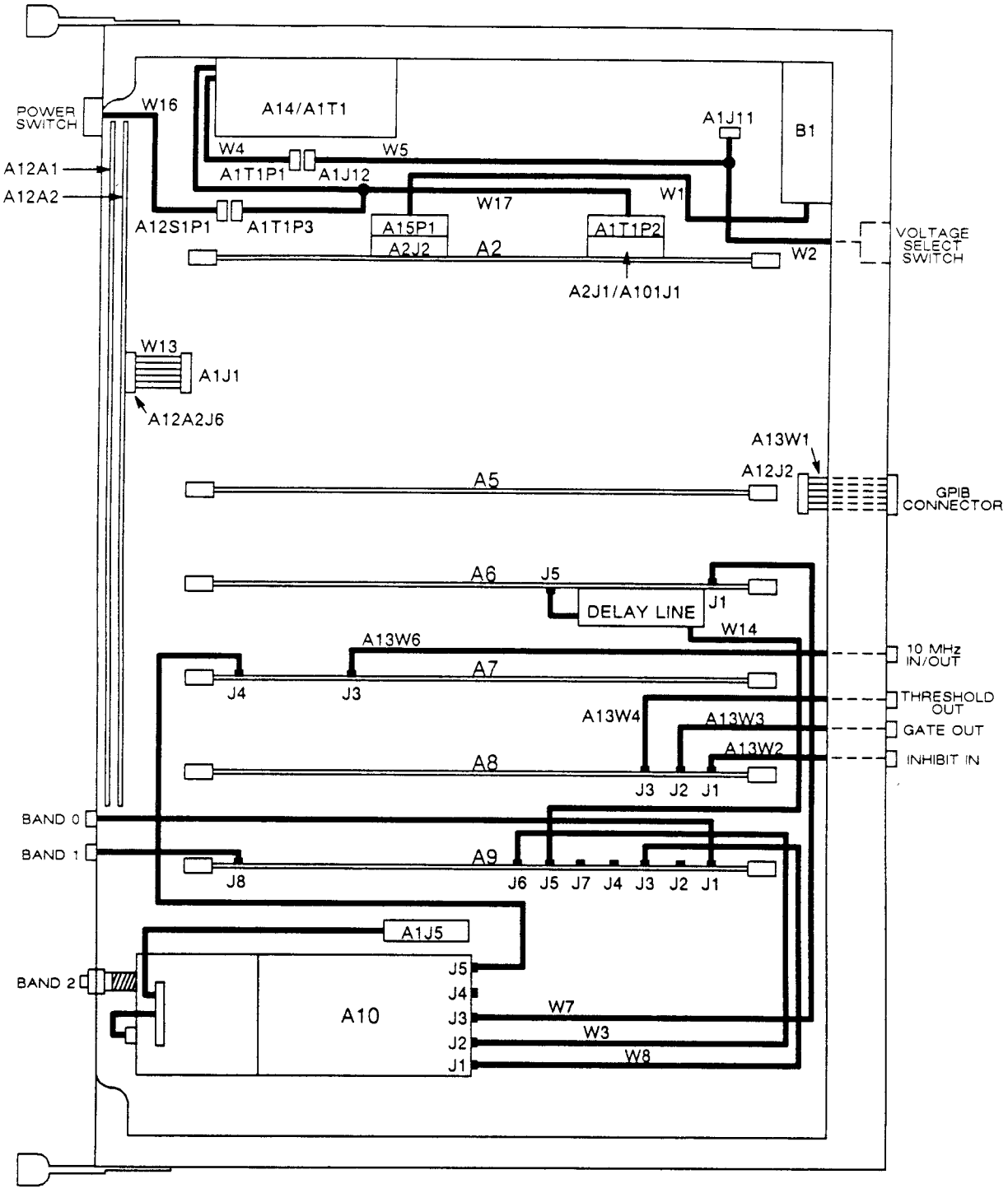

Figure 10-2. Counter Cable Assemblies.

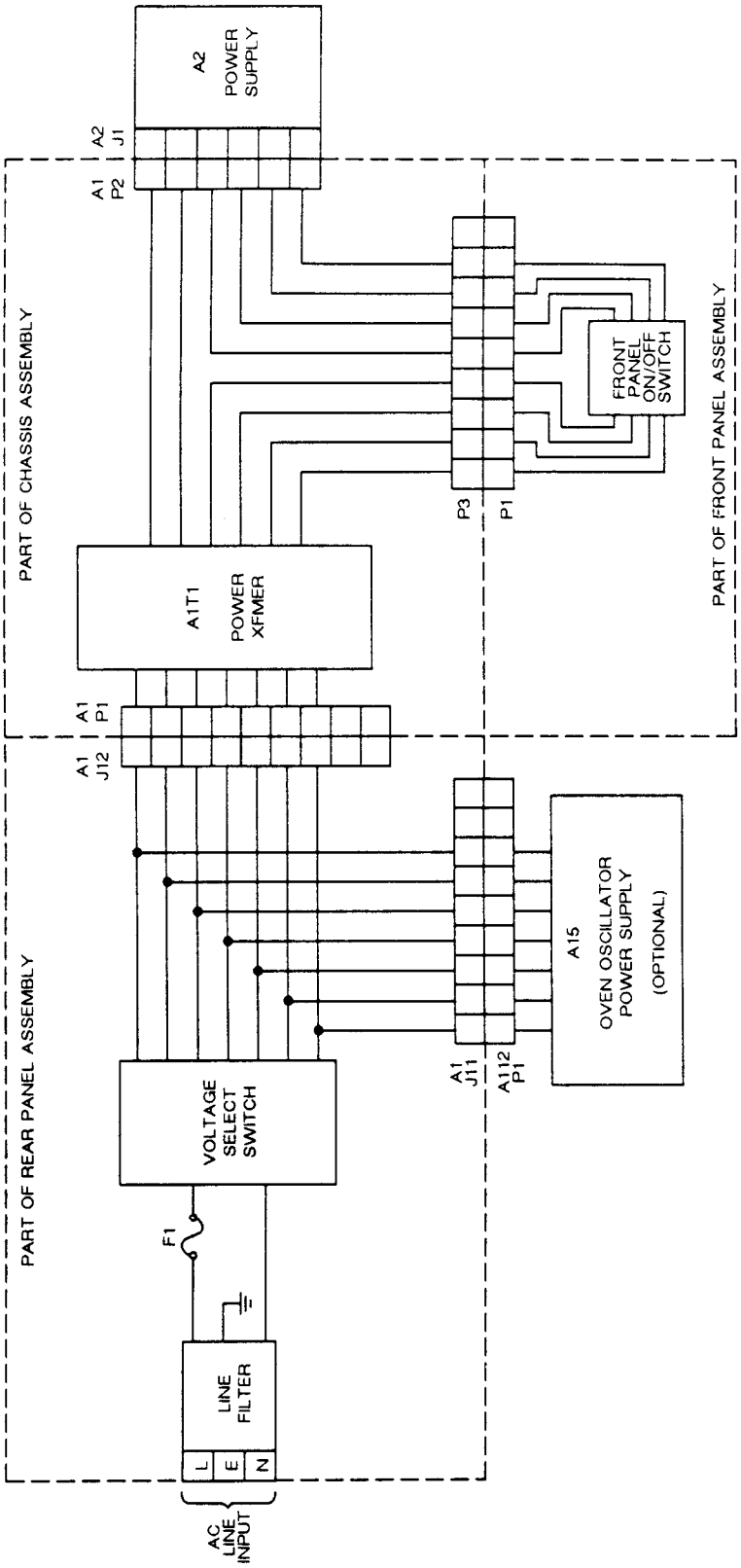

Figure 10-3. Power Entry Interconnect Diagram.

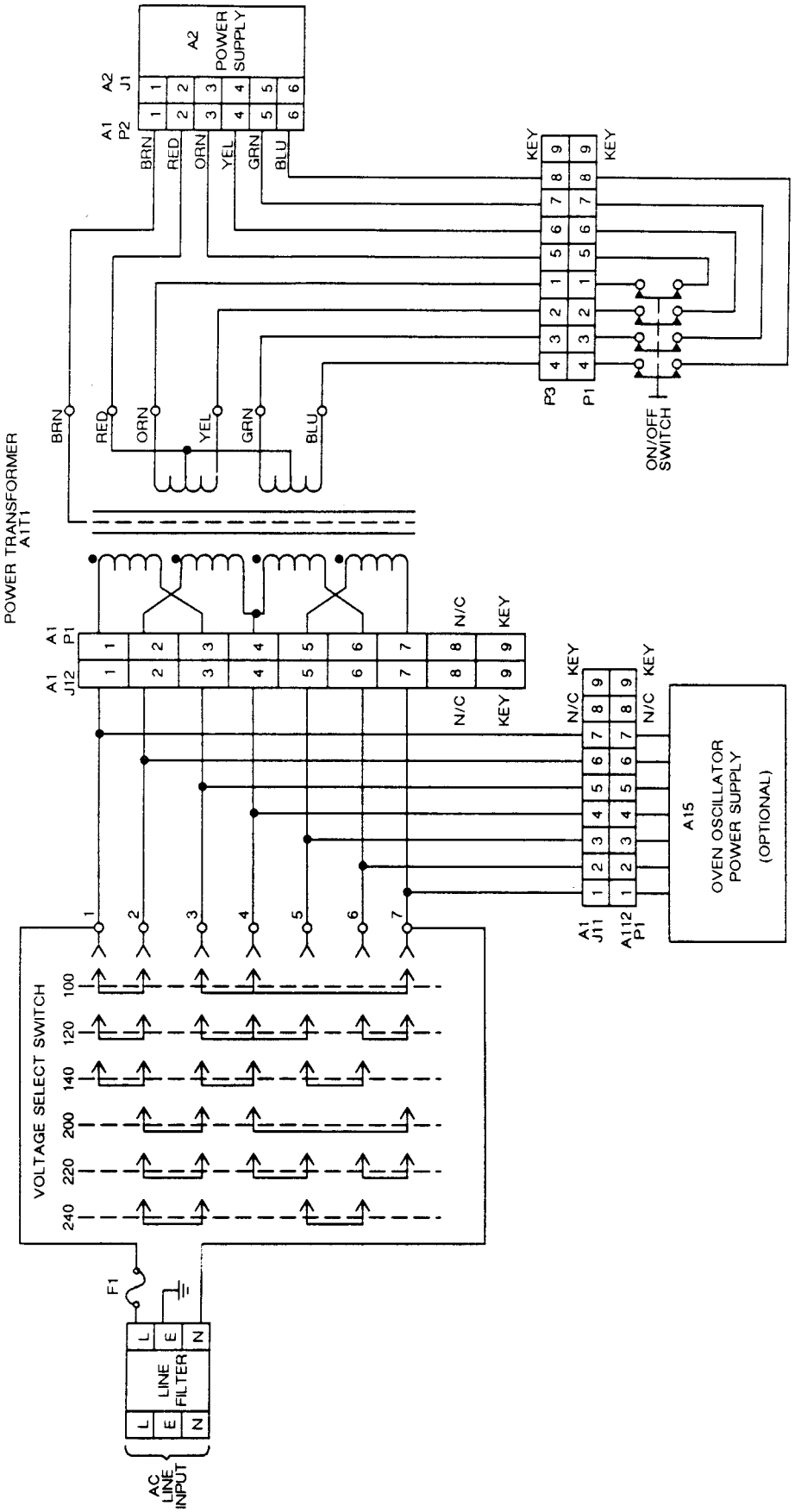

Figure 10-4. Power Entry Schematic Diagram.

A1
CHASSIS ASSEMBLY
2010772-02 Rev. A (585B)
2010768-02 Rev. A (588B)

ITEM NO.	DESCRIPTION	EIP NO.	UNITS PER ASSY
3	XFMR ASSY,PWR	2010755-01	1
5	FRAME,MOD,14IN,W/O HANDLES	5210248-02	2
6	CARD CAGE ASSY,TYPE 2	2010748-01	1
7	PCB ASSY,CNTR INTCON	2020406-01	1
13	PANEL,MICROWAVE SUPPORT	5201781-01	1
15	POST,COR,FRONT,BLK 2.70	5210430-02	2
16	POST,COR,REAR,BLK,2.70	5201431-02	2
17	PANEL,SIDE,VINYL CLAD,2.830	5210811-02	2
25	SCR,PNH X-REC 4-40X1/4 UNC	5120004-04	2
26	SCR,PNH,X-REC,SEMS,INTL,4-40X5/16	5171004-04	15
28	SCR,PNH X-REC SLFLKG 6-32X3/8 UNC	5124006-06	32
30	SCR,PNH X-REC SLFLKG 8-32X1/2 UNC	5124008-08	16
39	WASH,LK,INTL-T,CRES # 4	5163004-00	2
41	PAD,INSULATOR,SILICON TO-220	5000235-00	1
42	TIE,CABLE 0-.75 ID	5000093-00	1
43	IC,7805C,VOLT RGLTR,+5V,TO-220	3057805-02	1
44	HARN ASSY,REG,F/P	2040168-01	1
45	WASHER,FLAT,CRES NO.4	5160004-00	1
46	GROMMET,CATERPILLAR	5000122-00	2
47	STANDOFF,1/4 HEX,6-32X2.535LG	5100099-02	1
48	STANDOFF,1/4 HEX,6-32X2.560LG	5100099-03	1
49	SCR,PNH X-REC 6-32X1/2 UNC	5120006-08	2
50	GROMMET,CATERPILLAR,1/16"	5000355-00	5

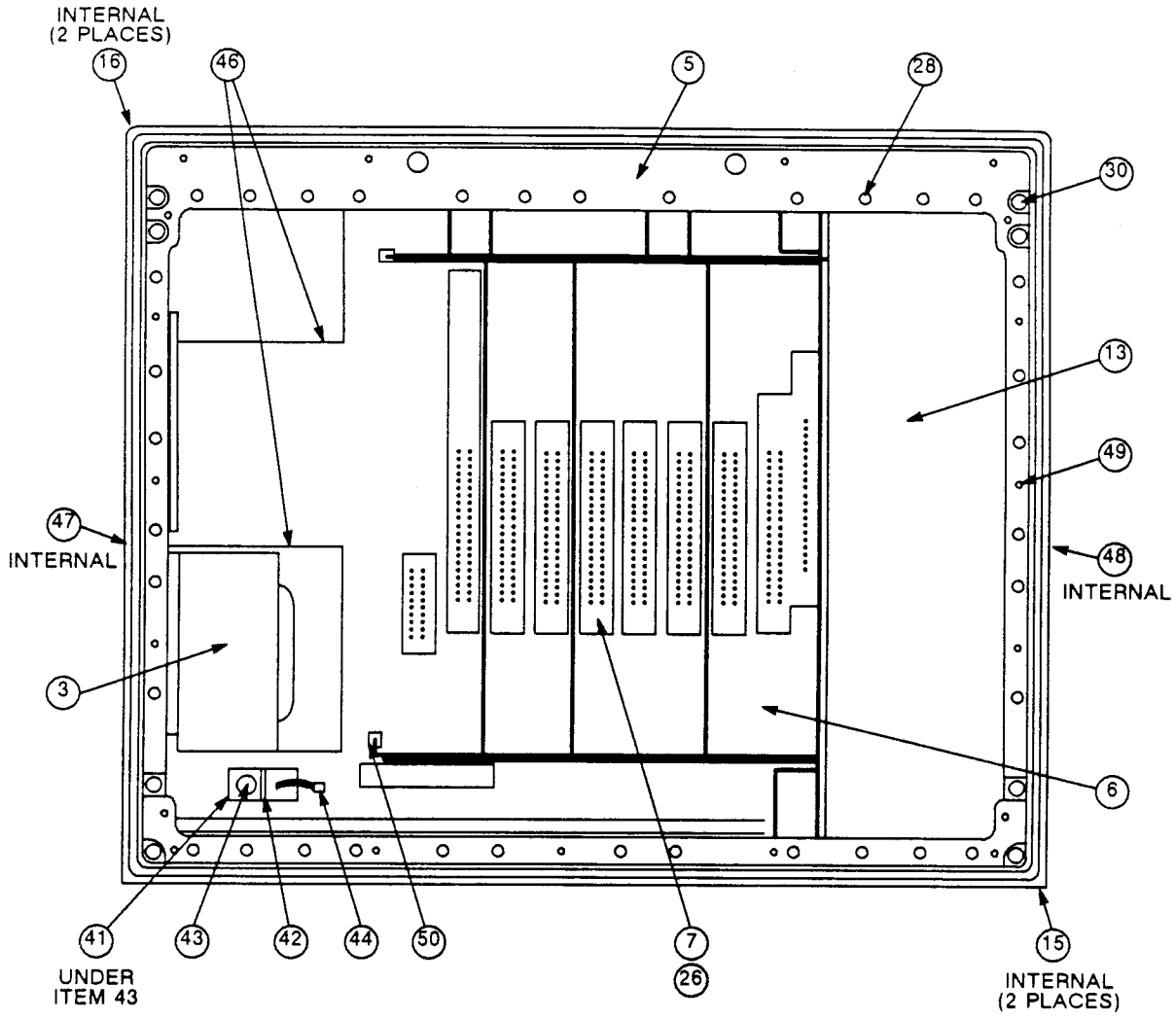

Figure 10-5. Chassis Assembly (A1) Replaceable Parts.

A1A1
COUNTER INTERCONNECT
(2020406-01 Rev. C)

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
J1		CONN,PCB HEADER,26 PIN,W/EJCTR	2620078-00	2
J2	J1			
J3		CONN,FRICT LK .156,6 PIN	2620090-00	1
J4		CONN,PCB,FRICT LK .156,10 PIN	2620092-00	1
J5		CONN,FRICT LK,HEADER,.156 13 PIN	2620151-00	1
XA1		NOT USED		
XA2		CONN,PCB EDGE,AMPL,22 PIN	2620183-00	1
XA3		NOT USED		
XA4		NOT USED		
XA5		CONN,PCB EDGE,60 PIN	2620184-00	5
XA6	XA5			
XA7	XA5			
XA8	XA5			
XA9	XA5			
HARDWARE USED IN THIS ASSEMBLY				
		PLUG,KEYING	5000155-00	5
		PCB SCHEMATIC DIAGRAM	5500406-01 B	REF.

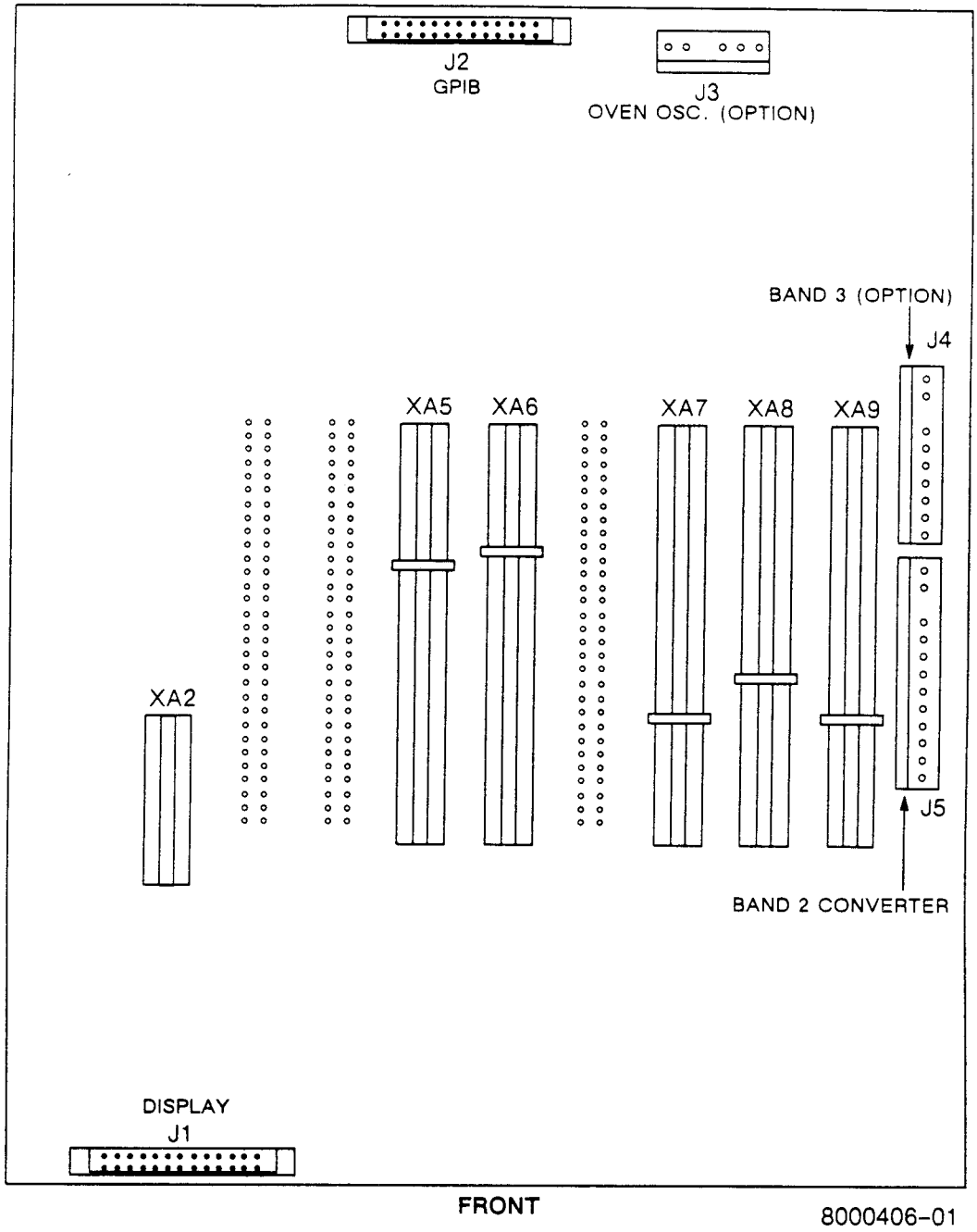

Figure 10-6. Counter Interconnect (A1A1) Component Locator.

J2
GPIB

OVEN OSC OPTION
J3

MILLIMETER WAVE
OPTION
J4

J5

POWER SUPPLY
XA2

XA3 SPARE

XA4 SPARE

XA5 PROCESSOR/
GPIB

XA6 COUNT CHAIN

XA6B SPARE

XA7 GATE
GENERATOR

XA8 GATE CONTROL

XA9 SIGNAL
CONDITIONER

MICROWAVE
CONVERTER

J1
FRONT
PANEL
DISPLAY

XX NO. FOR 30 PIN CONN.
(XX) NO. FOR 22 PIN CONN.

5500406-01 B

Figure 10-7. Counter Interconnect (A1A1) Schematic Diagram.

A2
POWER SUPPLY
(2020222-07)

The power supply furnishes all basic operating voltages required by the counter. The supply consists of two basic subassemblies.

- PCB (A2), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis-mounted components consisting of power transformer T1, primary wiring, fuse F1, the power programming switch, and the power control switch.

The basic voltages required by the counter are unregulated +18 V and +9 V and regulated +5 V, -5.2 V, +12 V and -12 V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of +9 V, -9 V, +18 V, and -18 V. A portion of the unregulated +18 V is used directly as one supply voltage for the microwave converter. The +18 V is also regulated to +12 V by an LM350T 3-terminal series regulator using thermal current protection, the -18 V is regulated to -12 V by a 3-terminal series regulator using thermal current protection.

The unregulated +9 V is applied to a +5 V regulator located on the chassis assembly adjacent to the front panel. This regulated +5 V is used to power the front panel logic and displays. The +9 V and -9 V unregulated supplies are also used for the +5 V and -5.2 V regulated supplies, each of which is regulated by a single 3-terminal regulator containing internal thermal and current shutdown circuitry.

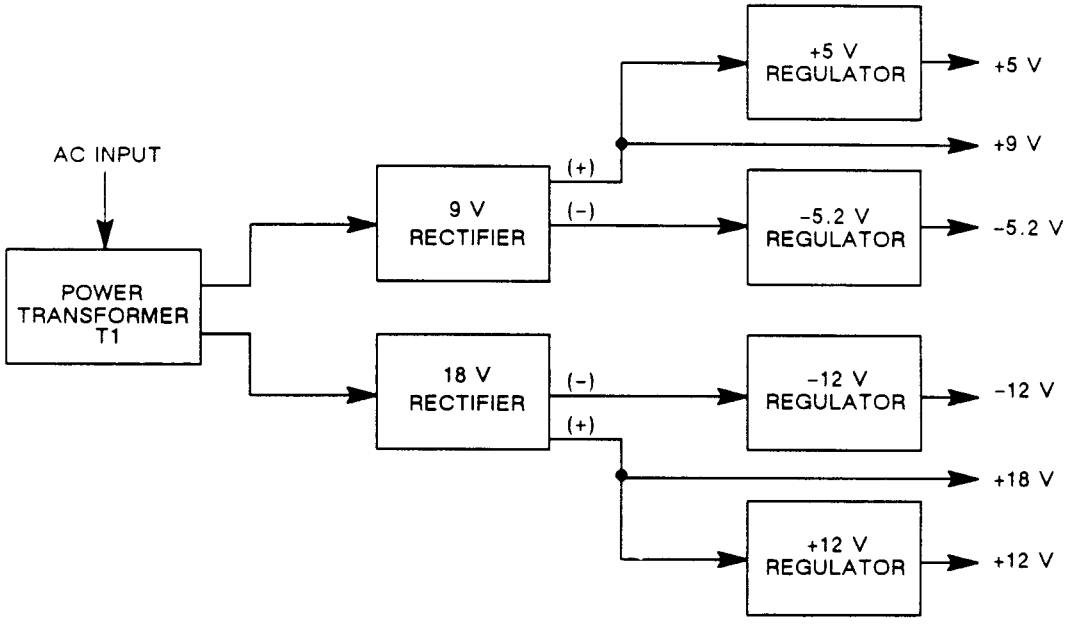

Figure 10-8. Power Supply Block Diagram.

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A2 POWER SUPPLY

2020222-07 Rev. C

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ELCTLT	32000µF	20%	15V	2200019-00	1
C2		CAP,ELCTLT	27000µF		15V	2200027-00	1
C3		CAP,TANTALUM	10µF	20%	25V	2300029-00	4
C4		CAP,ELCTLT	14000µF		25V	2200017-00	1
C5		CAP,ELCTLT	9500µF	20%	25V	2200016-00	1
C6	C3						
C7		CAP,TANTALUM	1µF		35V	2300008-00	3
C8	C3						
C9		CAP,TANTALUM	22µF		35V	2300034-00	1
C10	C3						
C11	C7						
C12	C7						
C13		CAP,ML CER	1µF	20%	50V	2150023-00	4
C14	C13						
C15	C13						
C16	C13						
CR1		DIODE,MDA970-2,BRIDGE,100V				2710045-00	1
CR2		DIODE,MDA990-1,BRIDGE				2710028-00	1
J1		CONN,SQ POST,6 PIN,156				2620157-00	1
J2		CONN,SQ POST,3 PIN,156				2620154-00	1
R1		RES,MF	475	1/10W	1%	4054750-00	1
R2		RES,MF	3.01K	1/8W	1%	4053011-00	1
R3		POT,CERMET	2.0	KT05	0.5W	4250016-00	2
R4		RES,CC	5.1	1W	5%	4030519-00	2
R5	R4						
R6	R3						
R7		RES,MF	8.66K	1/8W	1%	4068661-00	1
R8		RES,MF	1.21K	1/10W	1%	4051211-00	1
R9		RES,MF	200	1/4W	2%	4130201-00	1
R10		RES,CC	5.6	1/4W	5%	4010569-00	1
R11		RES,MF	13	1/4W	2%	4130130-00	1
R12		RES,CC	4.7	1/4W	5%	4010479-00	1
TP1		CONN,PIN-TP,SWAGE .040D-.150L				2620193-00	4
TP2	TP1						
TP3	TP1						
TP4	TP1						
U1		IC,78H05A,VOLT RGLTR,+5V,TO-3				3057805-01	1
U2		IC,LM350T,3A,RGLTR,ADJ,POS,TO-220				3040350-00	1
U3		IC,LM337,VOLT RGLTR,ADJ,NEG,TO-220				3040337-00	1
U4		IC,LM345-5.2,VOLT RGLTR,NEG,TO-3				3040345-00	1
HARDWARE USED IN THIS ASSEMBLY							
		HEATSINK,PWR SUPPLY				5210399-02	1
		PIN,ROLL,3/32 DIA 1/4 LG				5110008-00	2
		HANDLE,PCB				5230001-00	2
		PAD,INSULATOR,SILICON TO-220				5000235-00	2
		INSULATOR,SILICON TO-3				5000239-00	2
		BUSHING,NYLON INSUL				5000159-00	2
		SCR,PNH X-REC 6-32X3/4 UNC				5120006-12	1
		SCR,PNH X-REC 4-40X1/2 UNC				5120004-08	2

A2 POWER SUPPLY (Continued) 2020222-07 Rev. C

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
		WASHER,LK,INTL-5,CRES #4	5163004-00	2
		WASHER,FLAT,CRES,REDUCED O.D. #4	5161004-00	2
		WASHER,FLAT,FIBRE #4	5000136-00	1
		SCR,PNH,X-REC,SEMS,INTL,L6-32X1/4	5171006-04	3
		WASHER,LK,INTL-T,CRES #6	5163006-00	1
		WASHER,FLAT,CRES,REDUCED O.D. #6	5161006-00	1
		NUT,HEX,RES 4-40 UNC-2B	5180004-40	2
		WIRE,BUS,18 AWG	5460011-00	9.5
		TUBING,TEFLON 18 AWG CLR	5480012-00	8.5
		SCR,PNH,X-43C,SEMS,INTL,6-32X1/2	5171006-08	4
		NUT,HEX,CRES 6-32 UNC-2B	5180006-32	4
		WASHER,CONICAL OMPRESSION #6	5310032-00	4
		PCB SCHEMATIC DIAGRAM	5500222-07 A	REF.

Power Supply Component Locator
(PCB Assembly A2)

(See following page)

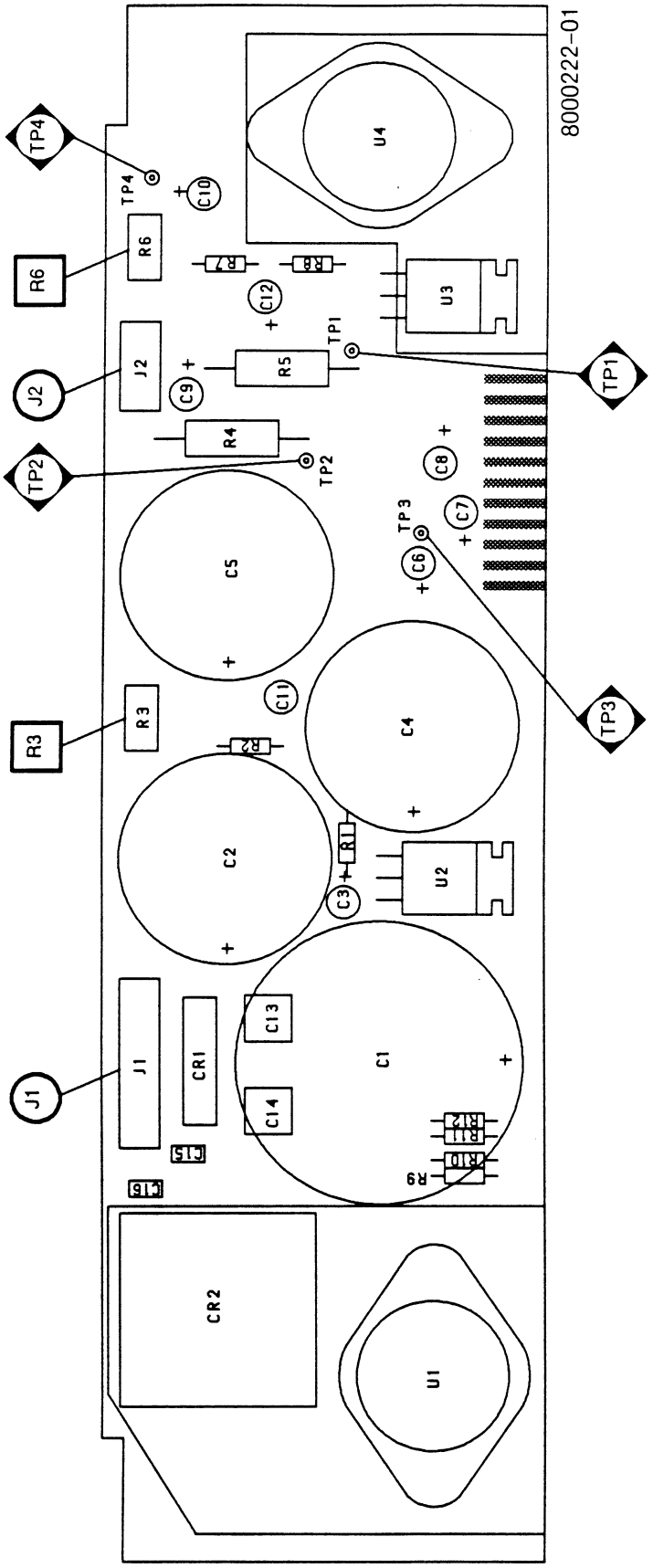
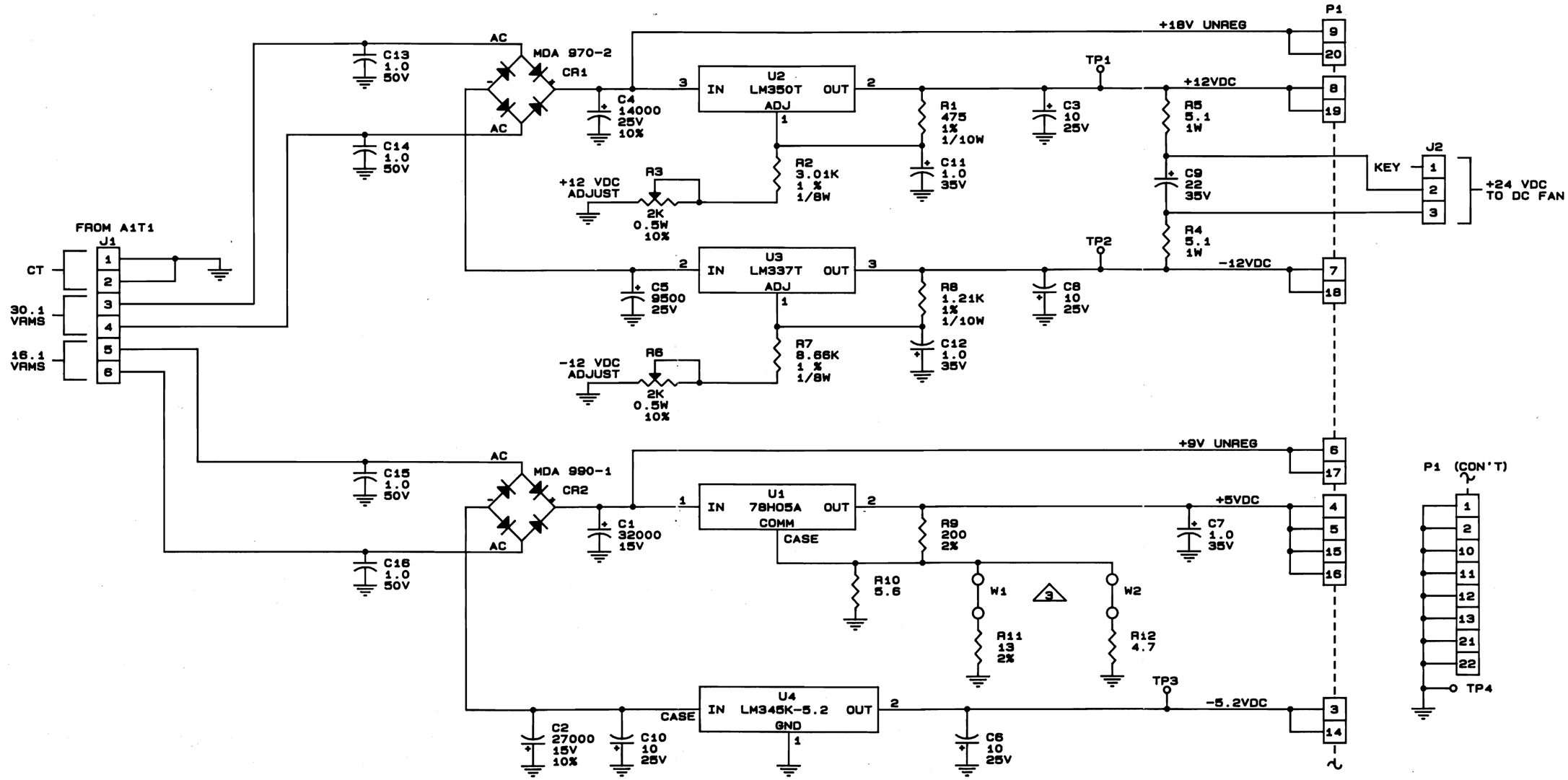


Figure 10-9. Power Supply (A2) Component Locator.



3 W1 AND W2 ARE USED TO ADJUST THE +5V OUTPUT.
2 ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS AND HAVE A TOLERANCE OF 20%.
1 ALL FIXED RESISTORS ARE 1/4 W, 5%. ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

5500222-07 A

Figure 10-10. Power Supply (A2) Schematic Diagram.

A5
PROCESSOR/GPIB
(2020400-02)

The processor/GPIB assembly contains the microprocessor, control logic, and firmware used to control counter operations along with the GPIB Interface circuitry. The processor portion of this assembly can be divided into five functional blocks:

- Microprocessor
- Power-on reset circuit
- Address decoder
- Counter memory
- Control logic and buffers

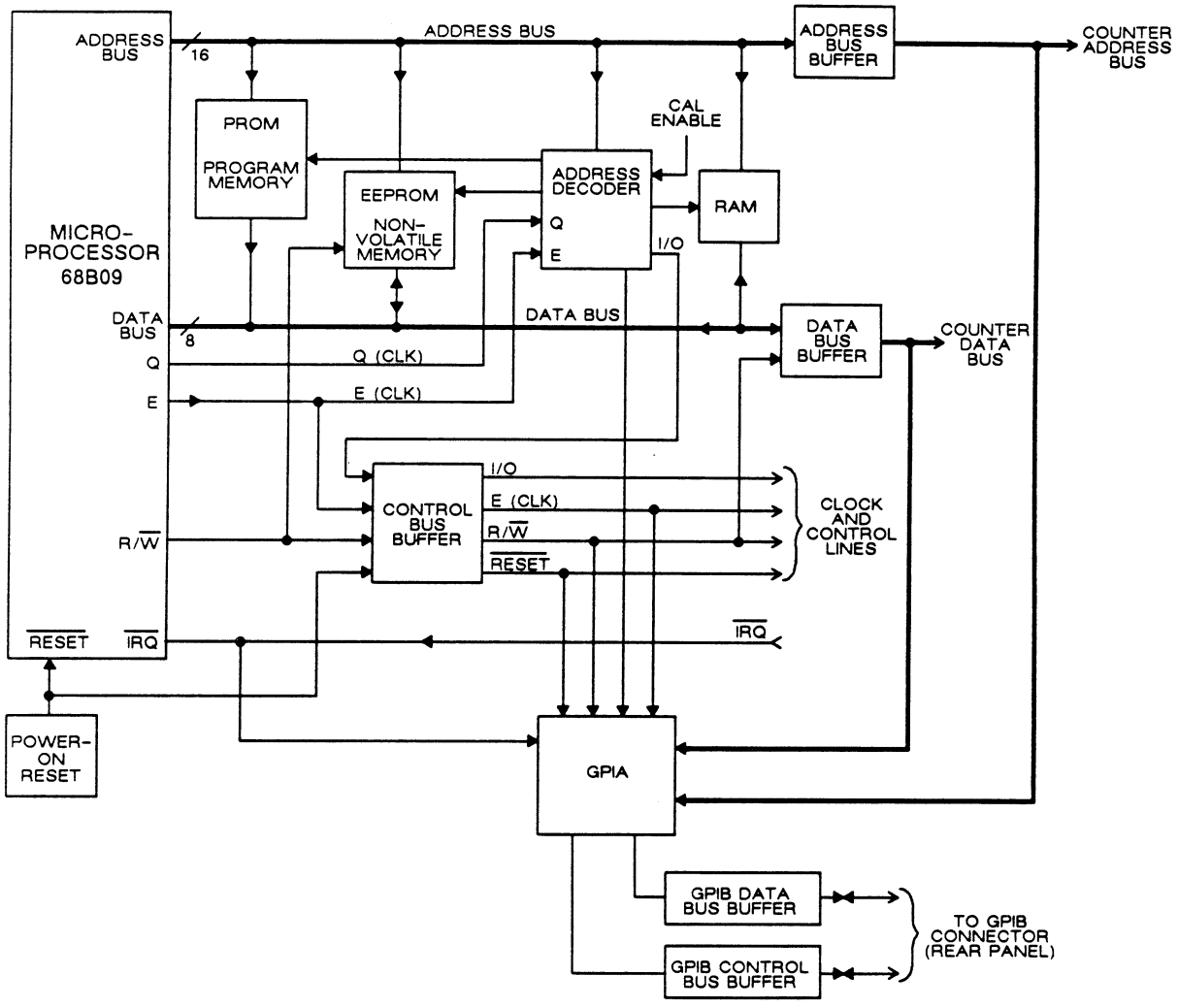


Figure 10-11. Processor/GPIB Simplified Block Diagram.

MICROPROCESSOR

The counter uses a Motorola 68B09 microprocessor (U12), which also contains the clock generation circuitry for the digital system. The NMI, FIRQ, and DMA functions of the 68B09 are not used, and their corresponding control lines are *always* disabled. The processor state indicators (BS and BA) also are not used. The $\overline{\text{IRQ}}$, $\overline{\text{HALT}}$, and MRDY control signals are connected through the edge connector to the counter interconnect board (A1A1).

POWER-ON RESET CIRCUIT

The power-on reset circuit, consisting of voltage comparator U13 and the associated circuitry, provides an active low reset signal for approximately 100 ms after the counter is first turned on. At turn-on, the voltage on U13 pin 3 is set to approximately 3.9 V by Zener diode CR1, and the voltage on pin 2 is low, which causes the output from U13 to be low. C17 slowly charges through R6 until the voltage on U13 pin 2 exceeds the voltage on pin 3. This causes the output from U13 to go from low to high, removing the reset condition. R4 provides hysteresis. When power is removed, C17 quickly discharges through CR2.

ADDRESS DECODER

Address decoding of the 64k byte address space is performed by programmable array logic (PAL) U5. The outputs from U5 enable the various memory devices depending on the input addresses of A9 through A15 and the status of the read/write (R/$\overline{\text{W}}$) line. U5 pin 15, CAL EN, is normally high to protect the portion of the EEPROM used for calibration tables. When performing calibration (Special Functions 91 and 92), this pin is grounded to allow information to be written to the calibration tables.

COUNTER MEMORY

The processor contains three types of memory: programmed read only memory (PROM), nonvolatile RAM (EEPROM), and RAM.

PROM MEMORY

The PROM memory contains the system program for the instrument, also known as instrument firmware. This program is contained in the upper 48k of a single 64k x 8 bit PROM (U9). Listed on the PROM is an EIP part number and a revision code that corresponds to the firmware contained in the particular instrument.

NONVOLATILE RAM

The 8k x 8 bit nonvolatile RAM (U2) contains temporary information that must be retained even if the unit is powered down. This type of information includes: stored instrument setups, calibration tables, GPIB address and unit configuration. The portion of this RAM that contains the calibration tables is normally protected to prevent the calibration information from being accidentally altered. During calibration a jumper is connected between U5 pin 15 and ground to allow information to be written to the protected portion of the memory.

RAM

The 8k x 8 bit volatile RAM (U6) is used as temporary memory during operation of the counter. The microprocessor uses this memory to store all temporary variables used in the operation of the instrument.

The following is the memory map of the instrument:

Volatile RAM Memory	0000 - 0FFF
Nonvolatile RAM Memory	3000 - 3FFF
I/O	1000 - 2FFF
Program Memory	4000 - FFEF
Reserved (68B09)	FFF0 - FFF1
SW13	FFF2 - FFF3
SW12	FFF4 - FFF5
FIRQ	FFF6 - FFF7
IRQ	FFF8 - FFF9
SWI	FFFA - FFFB
NMI	FFFC - FFFD
RESET	FFFE - FFFF

CONTROL LOGIC AND BUFFERS

The counter digital system contains three buses: the data bus, the address bus, and the control bus.

DATA BUS

The data bus originates in the microprocessor and is connected to the rest of the instrument via the main interconnect board. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing program header E1. The data bus on the microprocessor board is buffered from the rest of the digital system and is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/$\overline{W}$ control line.

ADDRESS BUS

The address bus also originates in the microprocessor and is connected to the rest of the instrument via the main interconnect board. The address bus buffers (U7 and U10) are always enabled.

CONTROL BUS

The control bus contains eight control lines, five of which originate in the processor board. The other three control lines originate in the rest of the digital system.

R/$\overline{W}$, E, and Q originate in the microprocessor. $\overline{RESET}$ is supplied by the power-up reset circuit. The I/O control line is true when A15 and A14 of U12 are at logic 0 and either A13 or A12 or both are at logic 1 levels. The $\overline{IRQ}$ control line is the wired-OR of all the interrupt request lines. MRDY is the wired-OR of all the memory ready control lines. The MRDY and $\overline{HALT}$ control lines are provided for future expansion.

GPIB INTERFACE

The GPIB interface makes the 585B and 588B counters fully compatible with IEEE 488 - 1978. The functions implemented are:

- Basic talker with talk only
- Basic listener
- Remote/local with local lockout
- Device clear
- Device trigger
- Service request

The general purpose interface adapter (GPIA) (U1) performs all the GPIB functions and protocols according to commands from the microprocessor. All data and messages between the microprocessor and the GPIB are transferred through U11.

Transceivers U2 and U3 provide the required bus buffering and termination for the GPIB. They are driven directly from the GPIA.

A5 PROCESSOR/GPIB 2020400-02 Rev. C

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ML CER	.01µF	10%	100V	2150014-00	13
C2	C1						
C3	C1						
C4	C1						
C5	C1						
C6	C1						
C7	C1						
C8	C1						
C9	C1						
C10	C1						
C11		CAP,TANTALUM	33µF		10V	2300015-00	1
C12	C1						
C13	C1						
C14		CAP,DISC,CER	22PF	10%	100V	2150067-00	2
C15	C14						
C16	C1						
C17		CAP,TANTALUM	3.9µF	10%	15V	2300027-00	1
CR1		DIODE,1N5228,ZENER 3.9V				2705228-00	1
CR2		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
E1		HEADER,PROGRAM DIP 16 PIN				5000205-00	1
R1		RES,MF	4.75K	1/8W	1%	4064751-00	4
R2	R1						
R3	R1						
R4		RES,MF	301K	1/8W	1%	4063013-00	1
R5		RES,MF	243	1/8W	1%	4062430-00	1
R6		RES,MF	22.1K	1/8W	1%	4062212-00	1
R7		RES,MF	1.00M	1/8W	1%	4061004-00	1
R8		RES,MF	30.1K	1/8W	1%	4063012-00	1
R9	R1						
RN1		RES,NTWK	9X10K	0.2W	2%	4170003-00	3
RN2	RN1						
RN3	RN1						
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	5
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
U1		IC,TMS9914A,GPIB CONTROLLER				3059914-00	1
U2		IC,X2864B,8KX8,EEPROM				6500042-01	1
U3		IC,75160A,GP INTERFACE BUS XCVR				3055160-00	1
U4		IC,75161				3050161-00	1
U5		PAL,PROGRAMMED,ADDRESS DECODER				2070085-02	1
U6		IC,HM6264P,8192X8BIT CMOS RAM				3000014-00	1
U7		IC,74LS244				3084244-00	2
U8		IC,74LS245				3084245-00	1
U9		SEE NOTE 1					
U10	U7						
U11		IC,74LS365				3084365-00	1
U12		IC,68B09,MP,8-BIT,2MHZ				3050025-00	1
U13		IC,LM311,VOLT COMPARATOR				3050311-00	1

NOTE 1: SEE TOP ASSEMBLY FOR PROGRAMMED PROM.

A5 PROCESSOR/GPIB (Continued) 2020400-02 Rev. C

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
W1		CONN,HEADER,2X2 PIN,.1 CTR	2620338-00	1
XE1		CONN,SOCKET,DIP,16 PIN	2630016-00	1
XU1		NOT USED		
XU2		NOT USED		
XU3		NOT USED		
XU4		NOT USED		
XU5		NOT USED		
XU6		NOT USED		
XU7		NOT USED		
XU8		NOT USED		
XU9		CONN,SOCKET,DIP,28 PIN	2630021-00	1
XY1		TIE,CABLE 0-.75 ID	5000093-00	1
Y1		CRYSTAL,4.000000MHZ	2030015-00	1
HARDWARE USED IN THIS ASSEMBLY				
		HANDLE,PCB	5230001-00	2
		PIN,ROLL,3/32 DIA 1/4 LG	5110008-00	2
		WIRE,INSUL,30 AWG,GREEN	5430555-00	1
		PCB SCHEMATIC DIAGRAM	5500400-02 B	REF.

Processor/GPIB Component Locator
(PCB Assembly A5)

(See following page)

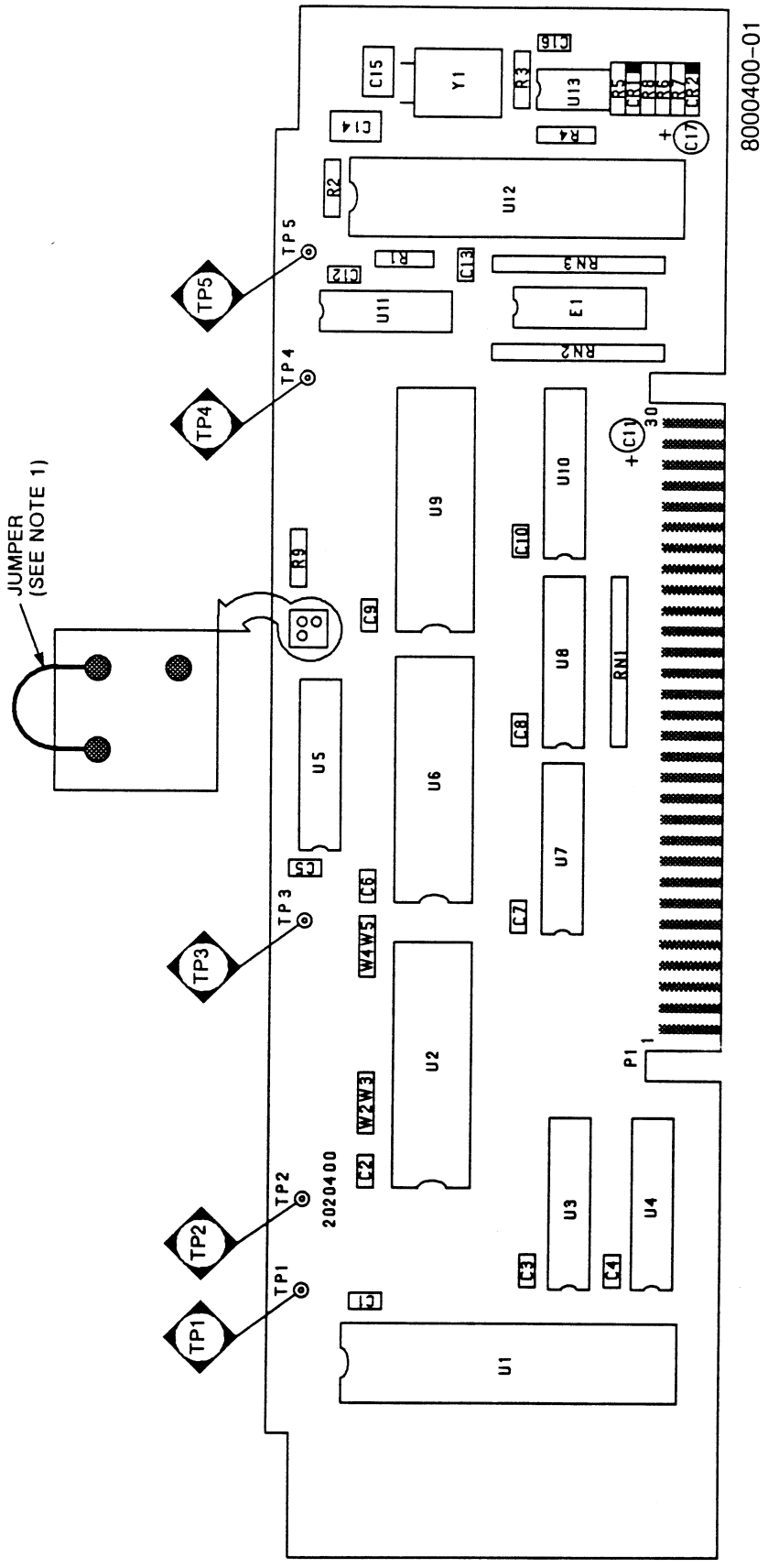


Figure 10-12. Processor/GPIB (A5) Component Locator.

NOTE 1: CONNECT JUMPER AS SHOWN BEFORE PERFORMING SPECIAL FUNCTIONS 46, 76, 91, AND 92. REMOVE JUMPER AFTER COMPLETION OF SPECIAL FUNCTIONS.

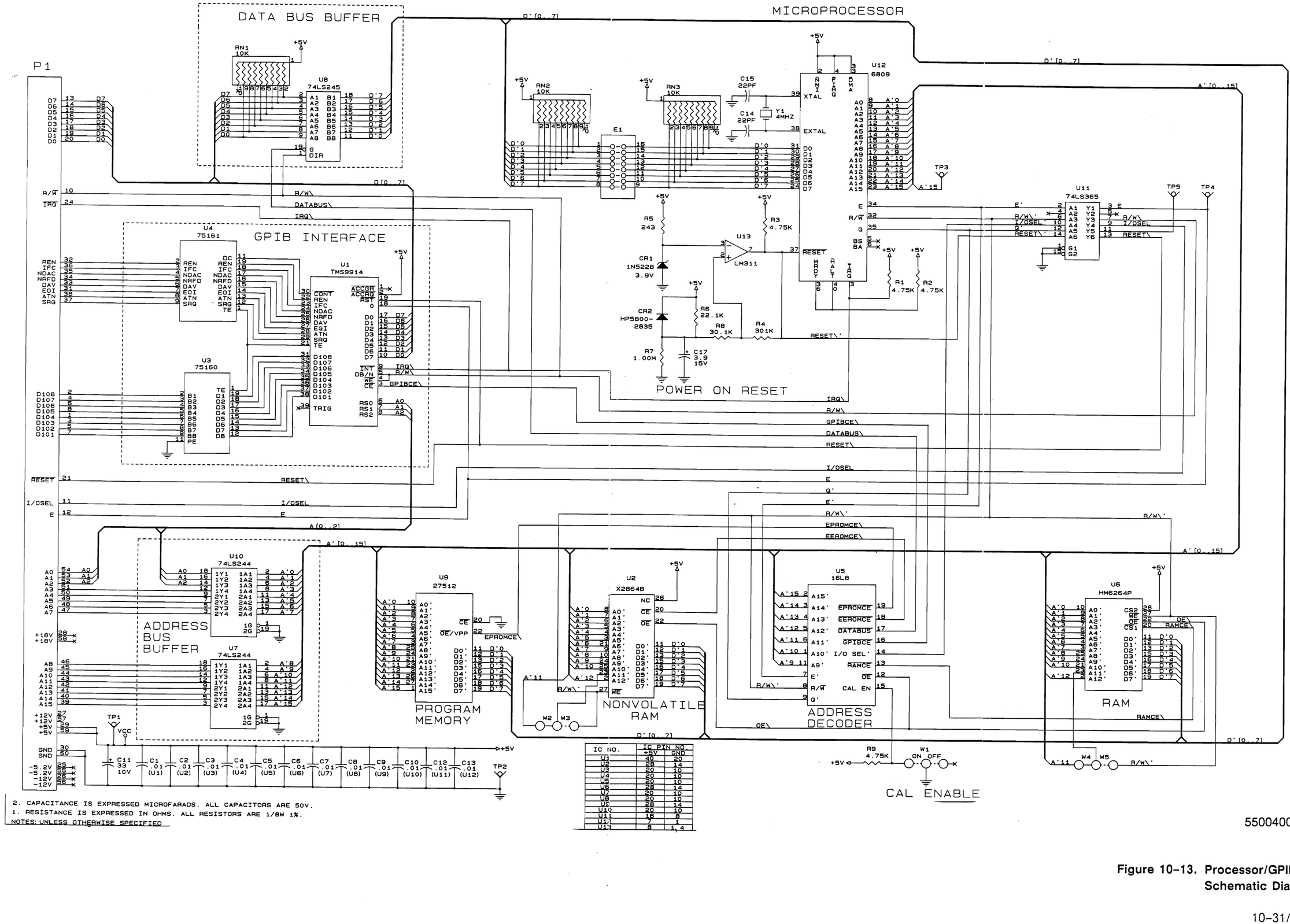


Figure 10-13. Processor/GPIB (A5) Schematic Diagram.

A5
PROCESSOR/GPIB
(2020480-02)

The Processor/GPIB assembly contains the microprocessor, control logic, and firmware used to control counter operations along with the GPIB interface circuitry. The processor portion of this assembly can be divided into five functional blocks:

- Microprocessor
- Power-on reset circuit
- Address decoder
- Counter memory
- Control logic and buffers

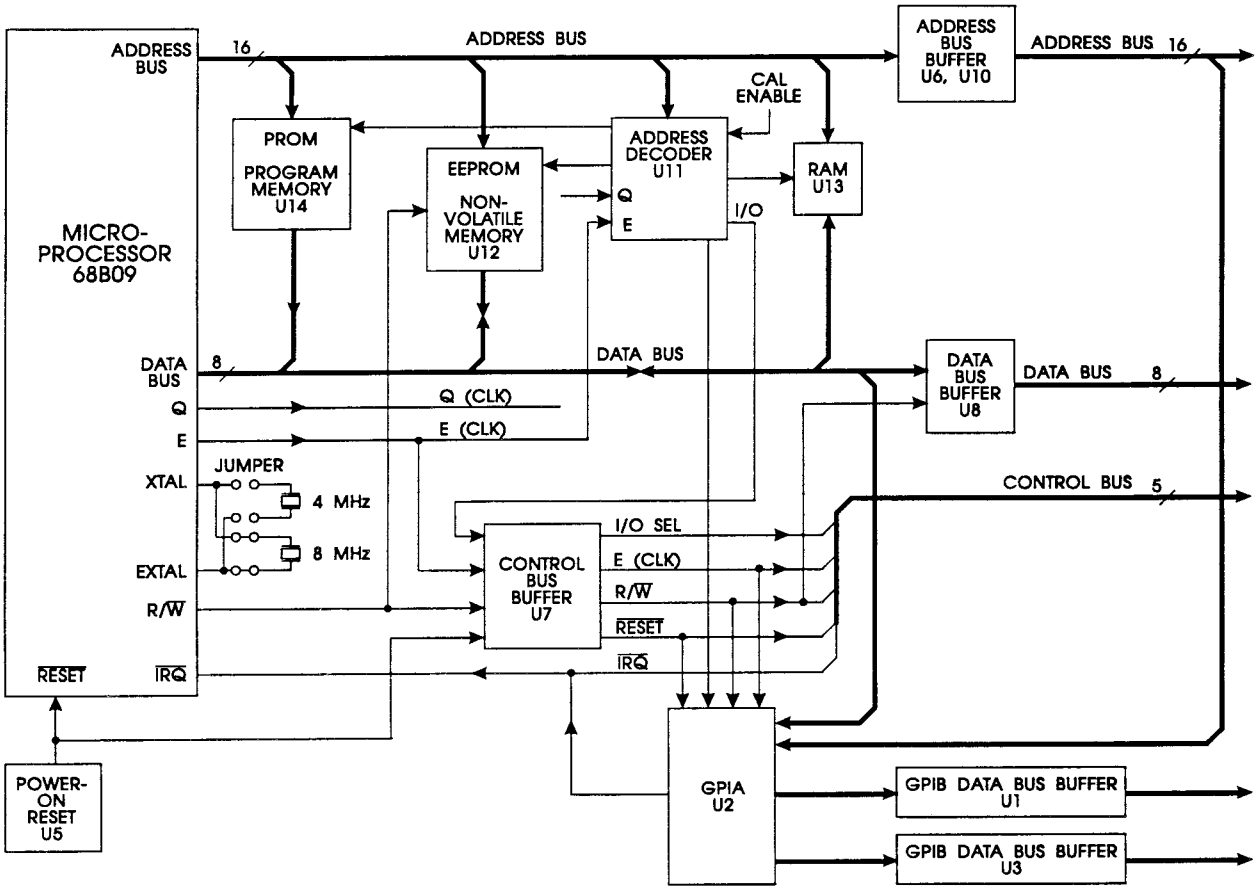


Figure 10-13A. Processor/GPIB Simplified Block Diagram.

MICROPROCESSOR

The Processor/GPIB assembly uses a Motorola 68B09 microprocessor (U4), which also contains the clock generation circuitry for the digital system. The only external components required for clock generation

are two 22 pF capacitors and either a 4 MHz (Y1) or 8 MHz (Y2) AT-cut crystal. The $\overline{NMI}$, $\overline{FIRQ}$, and $\overline{DMA}$ functions of the 68B09 are not used, and their corresponding control lines are always disabled. The processor state indicators (BS and BA) also are not used.

POWER-ON RESET CIRCUIT

The power-on reset circuit, consisting of a single chip (U5) and one filtering capacitor (C6), provides an active low reset signal for approximately 200 ms after the counter is first turned on. It also provides protection at power down. The power monitor chip (U4) has an internal precision voltage reference which is used to monitor +5 V supply and provide a fast reset when power is shut off which is achieved by sensing a drop in supply voltage. Since it takes a few milliseconds for the supply to go down, the power monitor chip has more than sufficient time to generate a reset and halt the processor before the supply line falls below approximately 4.4 volts.

ADDRESS DECODER

Address decoding of the 64K byte address space is performed by programmable array logic (PAL) U11. The outputs from U11 enable the various memory devices depending on the input addresses of A9 through A15 and the status of the read/write line, and E & Q clocks. U11 pin 15, CAL EN, is normally high to protect the portion of the EEPROM used for configuration and calibration tables. When configuring the counter or performing calibration (Special Function 91), this pin is grounded by placing a jumper on E5C (labeled as "CALENABLE") to allow the information to be written to the calibration tables.

COUNTER MEMORY

The processor contains three types of memory: programmed read only memory (PROM), nonvolatile RAM (EEPROM), and RAM.

PROM

The PROM memory contains the system program of the instrument, also known as instrument firmware. This program is contained in the upper 48K of a single 64K x 8 bit PROM (U14). Listed on the PROM is an EIP part number and a revision code that corresponds to the firmware contained in the particular instrument.

NONVOLATILE RAM

The 2K x 8 bit nonvolatile RAM or EEPROM (U12) contains temporary information that must be retained even if the unit is powered down. This type of information includes: calibration tables, GPIB address, and unit configuration. The portion of this EEPROM that contains the configuration and calibration tables is normally protected to prevent this information from being accidentally altered. During calibration, a jumper is connected to E5C labeled as "CALENABLE" to allow information to be written to the protected portion of the memory.

RAM

The 8K x 8 bit volatile RAM (U13) is used as temporary memory during operation of the counter. The microprocessor uses this memory to store all temporary variables used in the operation of the instrument.

CONTROL LOGIC AND BUFFERS

The Processor/GPIB assembly's digital system contains three buses: the data bus, the address bus, and the control bus.

DATA BUS

The data bus originates in the microprocessor and is connected to the rest of the instrument via the Counter Interconnect. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing program header E3 and installing it in E4 position (also labeled as "NOP"on the board). The data bus on the Processor board is buffered from the rest of the digital system in the counter via a bidirectional buffer (U8) and is enabled only when the address space assigned to I/O is addressed. The direction of the data buffer is determined by the state of the control line R/$\overline{W}$.

ADDRESS BUS

The address bus also originates in the microporcessor and is connected to the rest of the instrument via the Counter Interconnect. The address bus buffers (U6 and U10) are always enabled.

CONTROL BUS

The control bus contains eight control lines which originate on this assembly with the exception of the $\overline{IRQ}$ line. The $\overline{IRQ}$ control line is the wired-OR of all the interrupt request lines.

R/$\overline{W}$, Q, and E clock orginate in the microprocessor. RESET is supplied by the power-on reset circuit. The I/O control line is generated by the PAL (U11) when any I/O address range is addressed. The MRDY and $\overline{HALT}$ control lines are provided for future expansion.

GPIB INTERFACE

The GPIB interface makes the 585B and 588B counters fully compatible with IEEE 488 - 1978. The functions implemented are:

- Basic talker with talk only
- Basic listener
- Remote/local with local lockout
- Device clear
- Device trigger
- Service request

The general purpose interface adapter (GPIA) (U2) performs all the GPIB functions and protocols according to commands from the microprocessor. All data and messages between the microprocessor and the GPIB are transferred through U11.

Tranceivers U1 and U3 provide the required bus buffering and termination for the GPIB. They are driven directly from the GPIA.

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A5 PROCESSOR/GPIB 2020480-02 Rev. A

ITEM NO.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ML CER	.01µF	10%	100V	2150014-00	12
C2	C1						
C3	C1						
C4		CAP,DISC,CER	22PF	10%	100V	2150067-00	2
C5	C4						
C6		CAP,DISC,CER,X7R	.1µF	10%	50V	2150028-00	1
C7	C1						
C8	C1						
C9	C1						
C10	C1						
C11	C1						
C12		NOT USED					
C13	C1						
C14		CAP,TANTALUM	33µF	20%	10V	2300015-00	1
C15	C1						
C16	C1						
C17	C1						
E1		CONN,HEADER,2X8 PIN,DBL ROW,.1 CTR				2620227-00	3
E2	E1						
E3	E1						
E4		CONN,HEADER,8 PIN,0.1 CTR				2620316-00	2
E5	E5						
J1		CONN,PCB,RT ANGLE,26 PIN				2620131-00	1
R1		RES,M/OX	4.75K	1/8W	1%	4064751-00	4
R2	R1						
R3	R1						
R4	R1						
RN1		RES,NTWK,SIP	9X4.7K	.2W	2%	4170014-00	2
RN2	RN1						
U1		IC,75160A,GP INTERFACE BUS XCVR				3055160-00	1
U2		IC,TMS9914A,GPIB CONTROLLER				3059914-00	1
U3		IC,75161				3050161-00	1
U4		IC,68B09,MP,8-BIT,2MHZ				3050025-00	1
U5		IC,MAX694CPA, MP SUPERVISOR				3050037-00	1
U6		IC,74LS365				3084365-00	3
U7	U6						
U8		IC,74LS245				3084245-00	1
U9		NOT USED					
U10	U6						
U11		SEE NOTE 1					
U12		PROM,EE,2KX8				6400029-01	1
U13		IC,HM6264P,8192X8BIT CMOS RAM				3000014-00	1
U14		SEE NOTE 2					
XE1		CONN,JUMPER,2 PIN				2620304-00	1
XE2		CONN,JUMPER,2X2,.100				2620344-00	1
XE3		CONN, JUMPER,2X8,.100				2620343-00	1
XU1		NOT USED					
XU2		NOT USED					

NOTE 1: PART OF PROM SET. SEE TOP ASSEMBLY FOR PROM SET.
NOTE 2: SEE TOP ASSEMBLY FOR PROM SET.

A5 PROCESSOR/GPIB (Continued) 2020480-02 Rev. A

ITEM NO.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
XU3		NOT USED		
XU4		NOT USED		
XU5		NOT USED		
XU6		NOT USED		
XU7		NOT USED		
XU8		NOT USED		
XU9		NOT USED		
XU10		NOT USED		
XU11		CONN,SOCKET,DIP,20 PIN	2630018-00	1
XU12		CONN,SOCKET,DIP,24 PIN	2630020-00	1
XU13		NOT USED		
XU14		CONN,SOCKET,DIP,28 PIN	2630021-00	1
Y1		CRYSTAL,MP,HC-49,4.000 MHZ	2030154-00	1
Y2		CRYSTAL,MP,HC-49,8.000 MHZ	2030155-00	1
		PCB SCHEMATIC DIAGRAM	5500480-02	REF.
HARDWARE USED IN THIS ASSEMBLY				
		PIN,ROLL,3/32 DIA 1/4 LG	5110008-00	2
		HANDLE,PCB	5230001-00	2

Processor/GPIB Component Locator
(PCB Assembly A5)

(See following page)

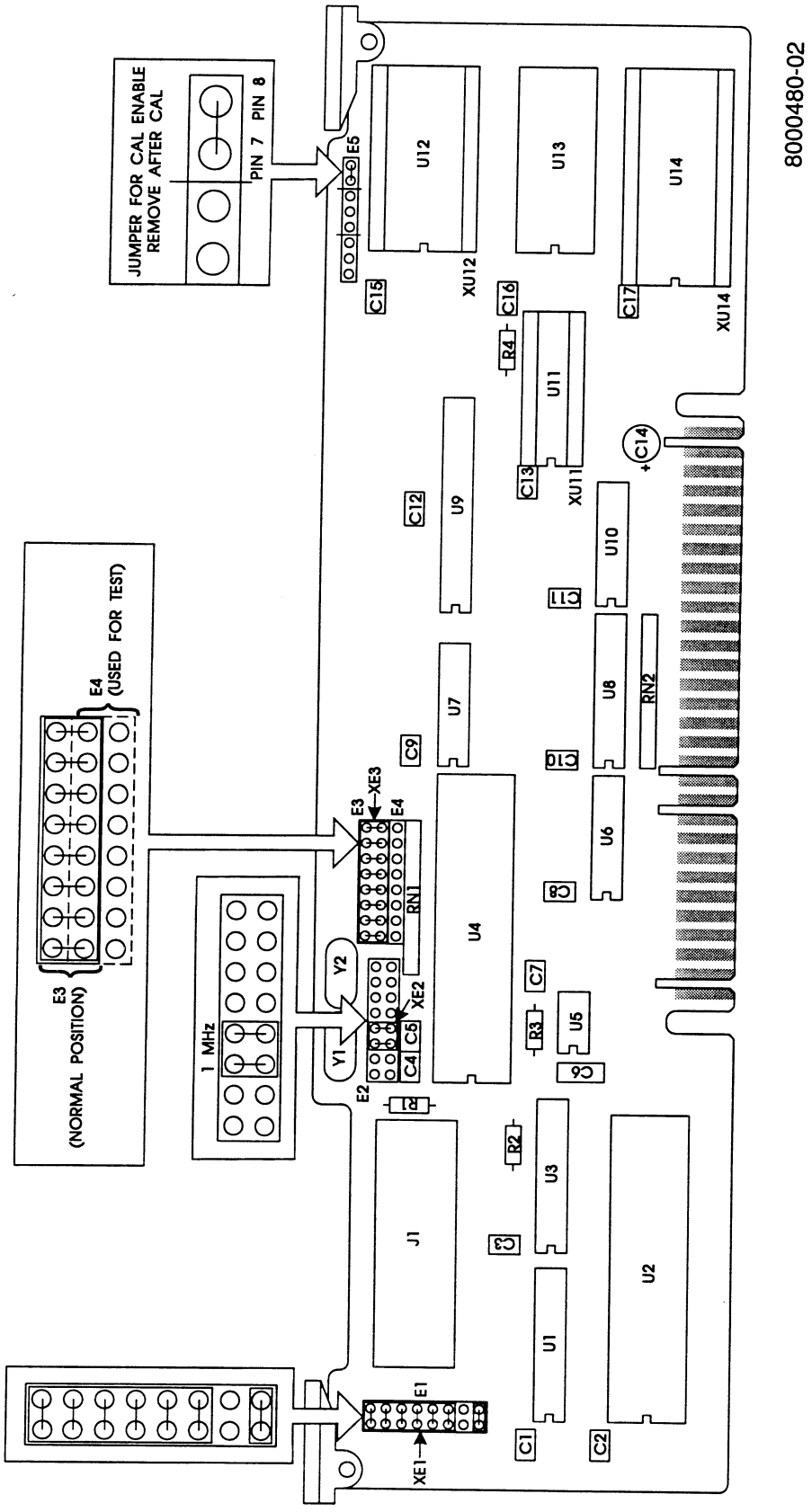
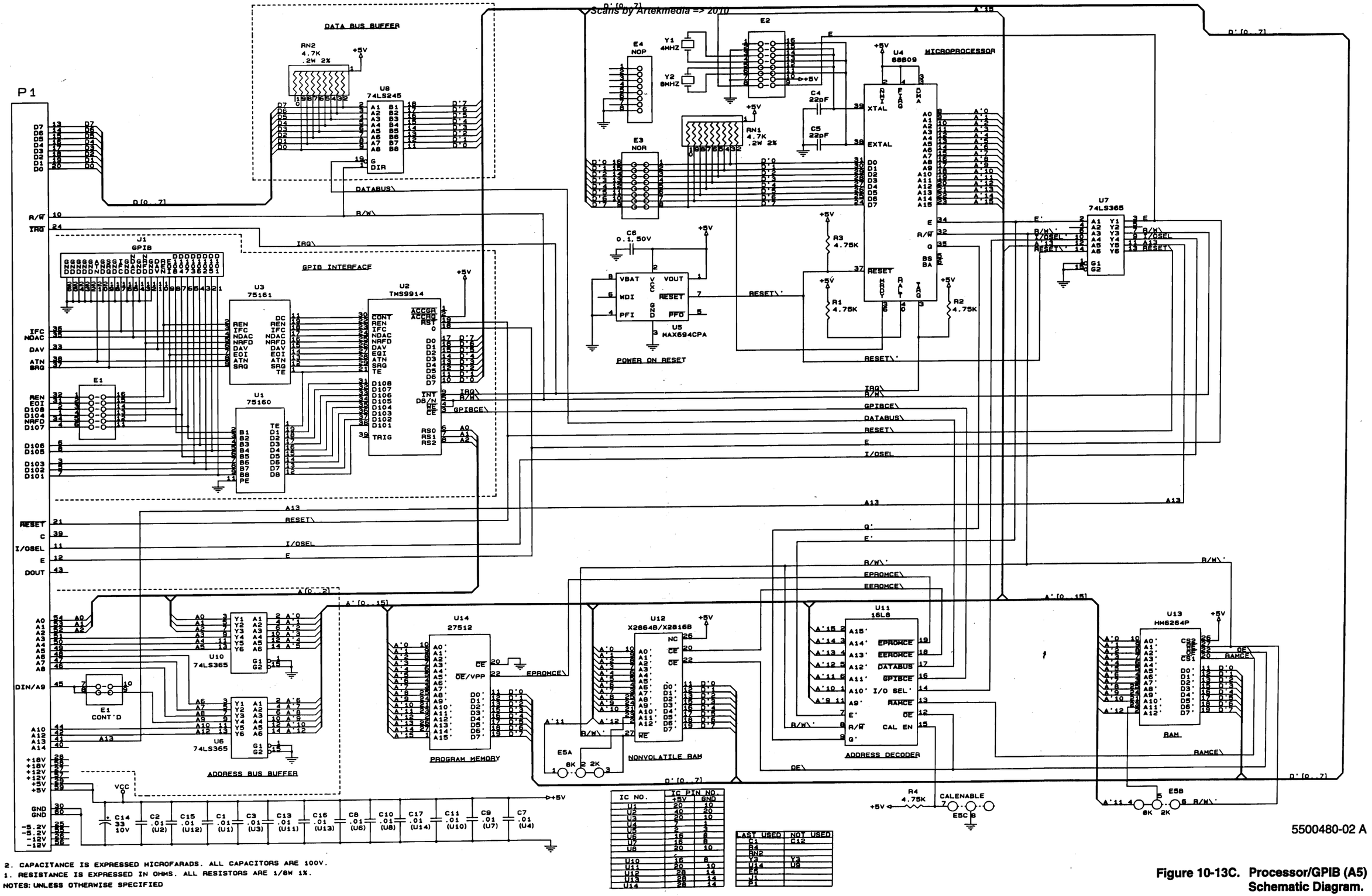


Figure 10-13B. Processor/GPIB (A5) Component Locator.



2. CAPACITANCE IS EXPRESSED MICROFARADS. ALL CAPACITORS ARE 100V.
1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W 1%.
NOTES: UNLESS OTHERWISE SPECIFIED

IC NO.	IC PIN NO. +5V	IC PIN NO. GND
U1	20	10
U2	40	20
U3	20	10
U4	6	1
U5	2	3
U6	16	8
U7	16	8
U8	20	10
U10	16	8
U11	20	10
U12	28	14
U13	28	14
U14	28	14

LAST USED	NOT USED
C1	C12
R4	
RN2	
Y2	
Y3	Y3
U14	U8
E5	
J1	
P1	

5500480-02 A

Figure 10-13C. Processor/GPIB (A5) Schematic Diagram.

A6
COUNT CHAIN
(2020404-01)

The primary function of the count chain is to count the number of zero crossings of an input signal in a given period of time, called the gate. The input signal may be the IF of the measured signal in the frequency mode, or the signal output by the VCO in the pulse parameter measurement and self-test modes. The count chain also provides the real-time clock for the counter.

The count chain assembly consists of the following functional blocks:

- IF delay circuit
- Divide-by-four prescaler
- IF pulse shaping network
- IF measurement
- Gate width adjustment
- Real-time clock

An IF/prescaler selector switch selects between the IF signal and the divide-by-four prescaler. Control and timing of the count chain board signals are performed by the processor board microprocessor through a peripheral interface adapter (PIA).

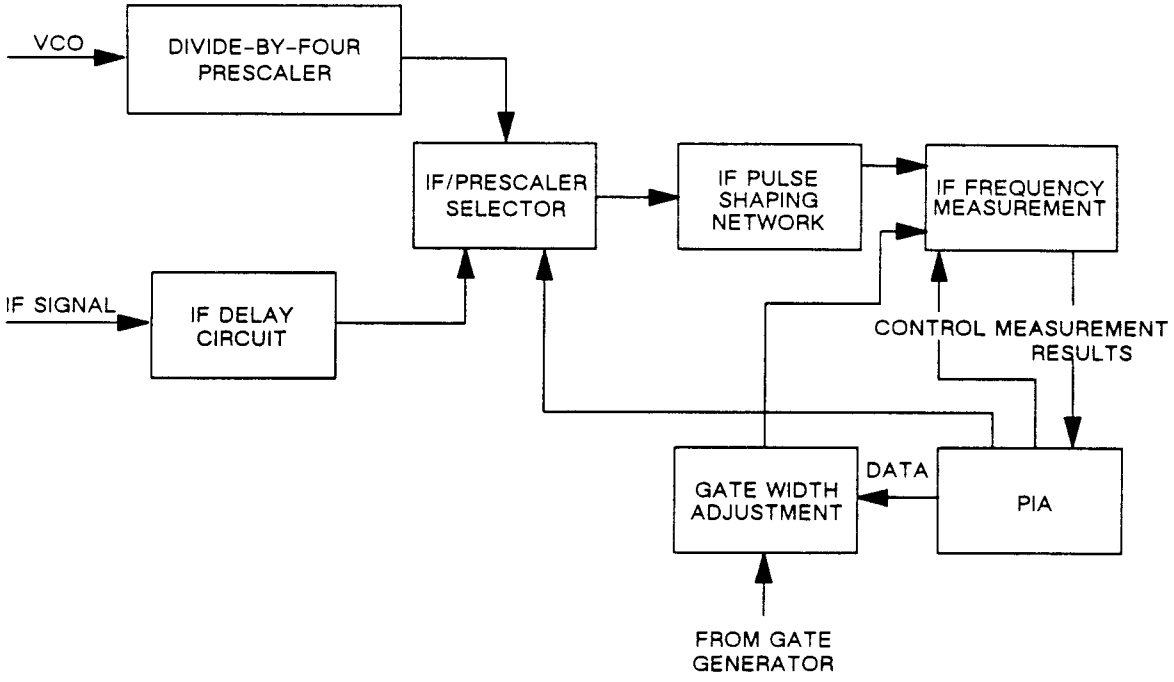


Figure 10-14. Count Chain Block Diagram.

SIGNAL PATH

The IF signal is applied to an IF delay circuit that delays the signal in order to adjust its timing to that of the gate signal. The gate signal is applied to the gate width adjustment circuit. There, it compensates for gate error and for minor changes in the gate width caused by passing the signal through the digital gates and the lines on the interconnect board.

When the counter is in the frequency measurement mode, the IF signal coming from the delay line passes through the IF/prescaler selector to the pulse shaping network. The waveform at this output consists of very short pulses (0.5 ns) at the point of zero crossing. The pulse shaping network output is applied to the gate input of the BCD counter in the IF measurement circuitry.

When the counter is in the pulse parameter measurement mode, the gate signal input to the IF/frequency measurement circuit is equal to the width or the period of the signal. The IF/prescaler selector is connected to the divide-by-four prescaler. Therefore the counter measures a known frequency of the VCO output divided by four, i.e., 100 to 125 MHz. The counter then computes the parameters according to the number of cycles it counts.

When the counter is in the test mode, the IF signal is fed from the divide-by-four prescaler at a constant frequency of 100 MHz.

IF DELAY CIRCUIT

The IF signal is directly connected to a 45 ns delay line consisting of approximately 30 feet of coax cable terminated with 50 ohms of resistance.

DIVIDE-BY-FOUR PRESCALER

The input to the divide-by-four IC (U1 pin 3) (through connector J1) is the output of the VCO, a 400 to 505 MHz CW signal that exists only in the self-test and pulse parameter modes of operation. The prescaler U1 divides the frequency by four and sends its output to U3 pin 10. Since U1 oscillates without any input, it is disabled by Q1 and R3. This resistor is floating when the counter is in either the self-test or the pulse parameter mode and Q1 is off, permitting U1 to divide.

When the counter is in the frequency measurement mode, R3 is connected to +12 volts via Q1, changing the bias condition of the divide-by-four prescaler and disabling the oscillation. It takes the divider approximately 10 μs to pass from an idle to a dividing state. The switching command is sent from the PIA (U13 pin 39) through U5A (pin 1), an open-collector TTL inverter.

IF PULSE SHAPING NETWORK

The IF signal from either the IF delay circuit or the divide-by-four prescaler is input to line receiver/differential amplifier U3 (pins 9 and 10 respectively). The output of U3 differentially drives wide band, high speed differential amplifier Q3 and Q4. The differential outputs of this amplifier drive current switch Q5. The resulting current square wave from Q5 drives inductor L2, producing a series of positive pulses when Q5 turns on and negative pulses when it turns off. These pulses are input to pulse inverter Q7 that acts as a high speed, zero crossing amplifier because it is biased at cutoff by Q9. (Q9 performs as a diode. It is the same type of

transistor as Q7 and is used for precise tracking over temperature.) Q7 inverts the positive pulses and removes the unwanted negative pulses. The pulse inverter output drives the input of the IF measurement circuitry (BCD counter).

IF MEASUREMENT

The IF measurement circuit consists of three major parts:

1. A divide-by-ten unit having BCD outputs (U7) and a surrounding bias circuit
2. An asynchronous 4 bit decade counter having BCD outputs (U11)
3. A 6-decade upcounter having 8-decade latches and a multiplexed BCD output (U12).

The IF measurement circuit derives its input frequency at U7 pin 14 of the pulse shaping network and its gate at U7 pin 16 of the gate width adjustment circuit. In response to microprocessor commands, it outputs the frequency readings at U12 pins 17, 18, 19, and 20.

The bias point for the U7 pin 14 input is established by a tracking bias circuit (U9 and Q6) whose output is equal to the voltage on U7 pin 1, plus a fixed dc voltage offset selected by resistors R62 and R63. This bias determines the threshold voltage of a U7 internal comparator.

The divide-by-ten output of the U7 decade counter is a 40/60 duty cycle ECL-level signal. It is converted to TTL by U10, an ECL-to-TTL translator, which, in turn, drives a second decade counter, U11.

The BCD outputs of U7 and U11 are connected to VLSI counter U12, which derives its clock information at pin 28 (B8) directly from the D output of U11 (pin 11). The TTL-compatible BCD outputs of U7 are very slow compared to the carry output (pin 9). As a result, these outputs will only settle to a defined state when the gate signal is removed.

When a count cycle is completed, eight decades of BCD data are read by the microprocessor (through PIA U13) by a time multiplex process. Multiplexer U12 (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the load clock (pin 21), and steps to the remaining seven digits with seven pulses on the scan clock line. A single reset line resets all count stages to zero before the next count cycle begins.

GATE WIDTH ADJUSTMENT

The gate width adjustment circuitry compensates for minute errors in the gate signal width caused by the digital circuitry. This is especially important in Band 1 and Band 3, where the higher frequency of the IF allows for greater frequency error. The gate signal enters the board on differential lines at the edge connector pins 6 and 36. The signal is input to U8A, a line receiver, whose output drives another line receiver acting as a differential inverting amplifier. The threshold signal for this second line receiver is derived from operational amplifier U15. Its output tracks the reference voltage on U8 pin 11 plus a fixed offset supplied by the voltage divider and digital-to-analog converter (DAC) consisting of U14 and U16. This accommodates slight changes in threshold that produce a change in gate width. The output of this circuit, consisting of U8 and U15, drives the clock enable input of U7 pin 16.

The DAC changes the bias in such a way that gate error can be corrected by software control. The error correction factors are stored in nonvolatile RAM. This enables automatic calibration of the gate signal.

REAL-TIME CLOCK

Real-time clock U17 delivers a 100 Hz square wave to PIA U13 pin 18. It is used for timing the flashing of the annunciators and for timing the intervals between loss of IF threshold checks.

IF/PRESCALER SELECTOR

When the IF signal is counted, the VCO signal is disabled by disabling U1. U1 is disabled by turning on Q1 through U5A which changes the bias on pin 3 of U1. The VCO signal is always present at J1, but no signal can pass through U1 in this mode.

When the VCO is counted, the IF signal is turned off from the signal conditioner board and, at the same time, U1 is enabled by disabling Q1, which removes the bias from pin 3 of U1.

A6 COUNT CHAIN

2020404-01 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ML CER	.01µF	10%	100V	2150014-00	10
C2	C1						
C3		CAP,ML CER	.001µF	10%	100V	2150015-00	16
C4	C3						
C5	C1						
C6	C3						
C7		WIRE,BUS,22AWG,.66 IN.				5460008-00	3
C8	C1						
C9	C7						
C10	C1						
C11	C3						
C12		NOT USED					
C13		NOT USED					
C14		NOT USED					
C15		NOT USED					
C16		NOT USED					
C17		NOT USED					
C18		NOT USED					
C19		NOT USED					
C20		NOT USED					
C21		NOT USED					
C22		CAP,SMD,CER,X7R	.01µF	10%	50V	2100040-00	4
C23	C1						
C24	C1						
C25	C22						
C26	C22						
C27		CAP,CHIP	.001µF	20%	50V	2100002-00	3
C28	C22						
C29	C27						
C30		CAP,TANTALUM	10µF	20%	25V	2300029-00	4
C31	C30						
C32	C3						
C33	C1						
C34		CAP,DISC,CER	33PF	10%	100V	2150069-00	3
C35	C3						
C36	C3						
C37		CAP,DISC,CER,X7R	.1µF	10%	50V	2150028-00	2
C38	C37						
C39	C1						
C40	C3						
C41	C3						
C42	C34						
C43	C3						
C44	C3						
C45	C34						
C46	C3						
C47	C3						
C48	C3						
C49	C3						
C50	C1						
C51	C3						
C52		CAP,TANTALUM	33µF		10V	2300015-00	4
C53	C52						
C54	C30						
C55	C30						
C56		NOT USED					
C57		NOT USED					
C58	C52						
C59	C27						
C60	C52						
C61		CAP,TANTALUM	100µF			2300024-00	1

A6 COUNT CHAIN (Continued) 2020404-01 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
CR1	C7						
CR2		DIODE,1N5234,ZENER 6.2V				2705234-00	1
CR3		DIODE,1N5231,ZENER 5.1V				2705231-00	1
CR4		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
DL1		DELAY LINE ASSY,58XB				2010800-01	1
J1		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	3
J2		NOT USED					
J3		NOT USED					
J4		NOT USED					
J5	J1						
J6	J1						
L1		INDUCTOR,1.0UH				3510003-00	1
Q1		XSTR,2N4126,PNP,GP				4704126-00	1
Q2		NOT USED					
Q3		XSTR,NE02137,NPN,MICROWAVE				4710032-00	5
Q4	Q3						
Q5		XSTR,MRF536,PNP,RF				4710044-00	2
Q6	Q3						
Q7	Q3						
Q8	Q5						
Q9	Q3						
R1		RES,MF	51	1/4W	2%	4130510-00	3
R2		RES,MF	1K	1/4W	2%	4130102-00	13
R3		RES,MF	10K	1/4W	2%	4130103-00	4
R4		RES,MF	330	1/4W	2%	4130331-00	7
R5		RES,CC	5.6	1/4W	5%	4010569-00	8
R6		NOT USED					
R7		NOT USED					
R8		NOT USED					
R9	R1						
R10		RES,MF	100	1/4W	2%	4130101-00	2
R11	R2						
R12	R3						
R13		NOT USED					
R14		NOT USED					
R15		NOT USED					
R16		NOT USED					
R17		NOT USED					
R18		NOT USED					
R19		NOT USED					
R20	R4						
R21		NOT USED					
R22		NOT USED					
R23		NOT USED					
R24		RES,MF	130	1/4W	2%	4130131-00	2
R25		RES,MF	56	1/4W	2%	4130560-00	2
R26	R24						
R27		RES,MF	430	1/4W	2%	4130431-00	1
R28	R5						
R29	R25						
R30		NOT USED					
R31	R4						
R32		NOT USED					
R33		NOT USED					
R34		NOT USED					
R35		NOT USED					
R36	R2						

A6 COUNT CHAIN (Continued) 2020404-01 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R37	R2						
R38	R5						
R39		RES,MF	39	1/4W	2%	4130390-00	2
R40	R4						
R41	R2						
R42		NOT USED					
R43		RES,MF	10	1/4W	2%	4130100-00	1
R44		RES,MF	510	1/4W	2%	4130511-00	1
R45		RES,MF	47	1/4W	2%	4130470-00	1
R46	R39						
R47	R5						
R48	R2						
R49		NOT USED					
R50		NOT USED					
R51		NOT USED					
R52		NOT USED					
R53		NOT USED					
R54		NOT USED					
R55	R2						
R56		RES,MF	220	1/4W	2%	4130221-00	1
R57	R10						
R58		RES,MF	20K	1/4W	2%	4130203-00	4
R59	R58						
R60	R58						
R61	R58						
R62	R2						
R63		RES,MF	33	1/4W	2%	4130330-00	1
R64	R2						
R65		RES,MF	240	1/4W	2%	4130241-00	2
R66	R65						
R67	R3						
R68	R4						
R69	R2						
R70	R3						
R71	R5						
R72		NOT USED					
R73		NOT USED					
R74	R2						
R75		NOT USED					
R76	R5						
R77	R5						
R78		RES,MF	8.2K	1/4W	2%	4130822-00	1
R79		RES,MF	750K	1/4W	2%	4130754-00	1
R80	R5						
R81	R1						
R82	R2						
R83	R4						
R84		RES,MF	270	1/4W	2%	4130271-00	1
R85	R2						
R86		NOT USED					
R87		NOT USED					
R88		NOT USED					
R89	R4						
R90		NOT USED					
R91		RES,MF	82	1/4W	2%	4130820-00	2
R92	R92						
RN1		NOT USED					
RN2		RES,NTWK	7X330	.8W	2%	4170010-00	1
RN3		RES,NTWK	5X330		2%	4170012-00	1
RN4		RES,NTWK	7X10K	0.3W	2%	4170004-00	1

A6 COUNT CHAIN (Continued) 2020404-01 Rev. E

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
TP1		CONN,PCB,.040D PIN,GOLD	2620032-00	9
TP2	TP1			
TP3	TP1			
TP4	TP1			
TP5	TP1			
TP6		NOT USED		
TP7	TP1			
TP8	TP1			
TP9	TP1			
TP10	TP1			
U1		IC,3199E,VHF/UHF,4 PRESCALER	3043199-00	1
U2		NOT USED		
U3		IC,10H116,ECL 10KH,LINE RCVRS	3118116-00	1
U4		NOT USED		
U5		IC,7406	3007406-00	1
U6		NOT USED		
U7		IC,HIGH SP DEC COUNTER	3018634-00	1
U8		IC,10216,ECL 10K,HI SP LINE RCVR	3110216-00	1
U9		IC,LM308A,OPNL AMP/BUFFER	3040308-00	3
U10		IC,10125,ECL 10K,TRANSLATORS	3110125-00	1
U11		IC,74LS160	3084160-00	1
U12		IC,7031,CNTR,6-DECADE,UP,PMOS	3057031-00	1
U13		IC,6820,PIA	3086820-00	1
U14		IC,AD7524J,DAC,8-BIT,1/2 LSB	3057524-00	1
U15	U9			
U16	U9			
U17		IC,555,TIMER	3040555-00	1
HARDWARE USED IN THIS ASSEMBLY				
		HANDLE,PCB	5230001-00	2
		PIN,ROLL,3/32 DIA 1/4 LG	5110008-00	2
		SCR,PNH X-REC 6-32X1 3/8 UNC	5120006-22	1
		WASHER,FLAT,CRES,REDUCED O.D. #6	5161006-00	1
		NUT,HEX,SM-PATT,CRES 6-32 UNC-2B	5182006-32	1
		WASHER,LK,INTL-T,CRES #6	5163006-00	1
		WIRE,BUS,22 AWG	5460008-00	2
		PCB SCHEMATIC DIAGRAM	5500404-01 E	REF.

Count Chain Component Locator
(PCB Assembly A6)

(See following page)

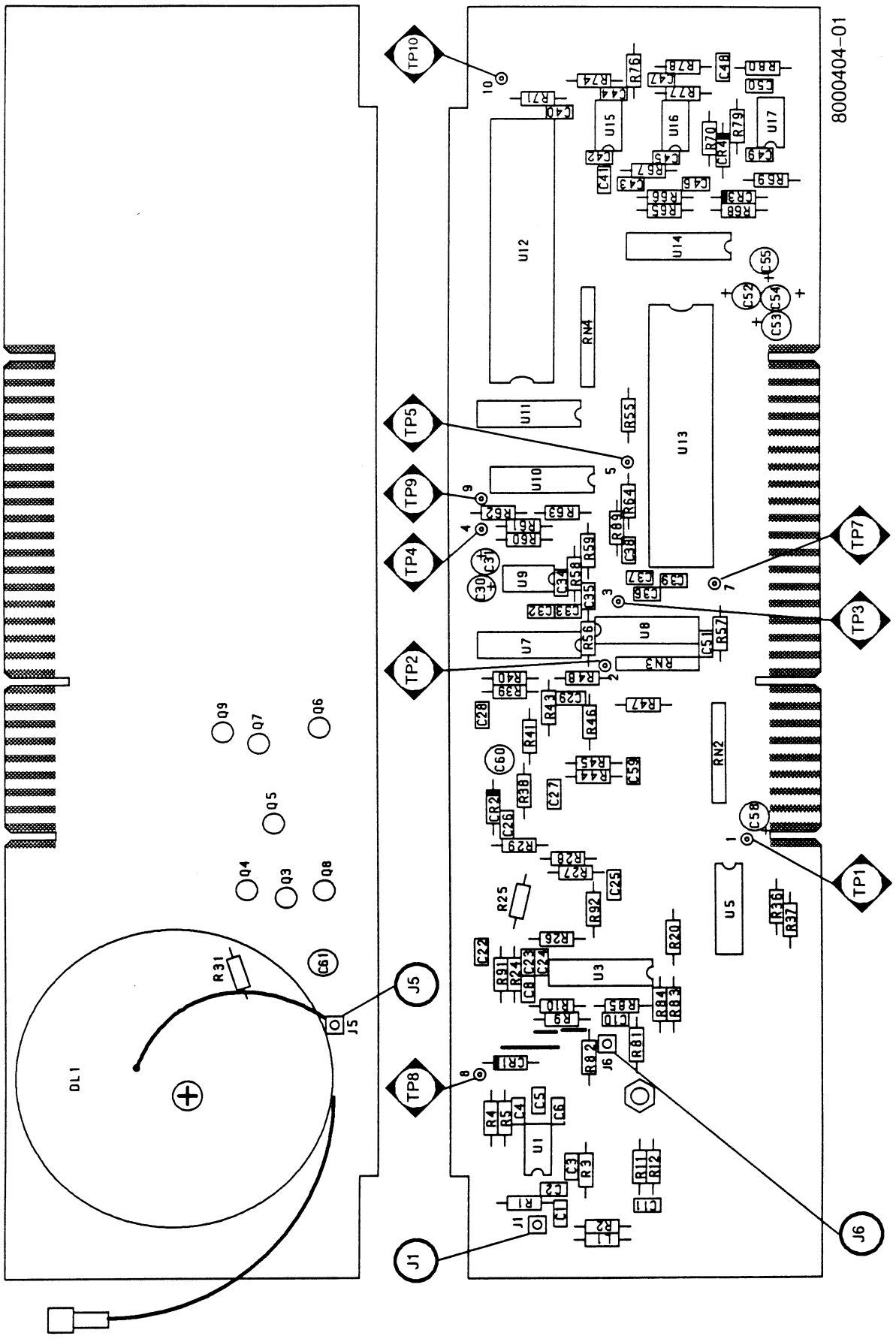
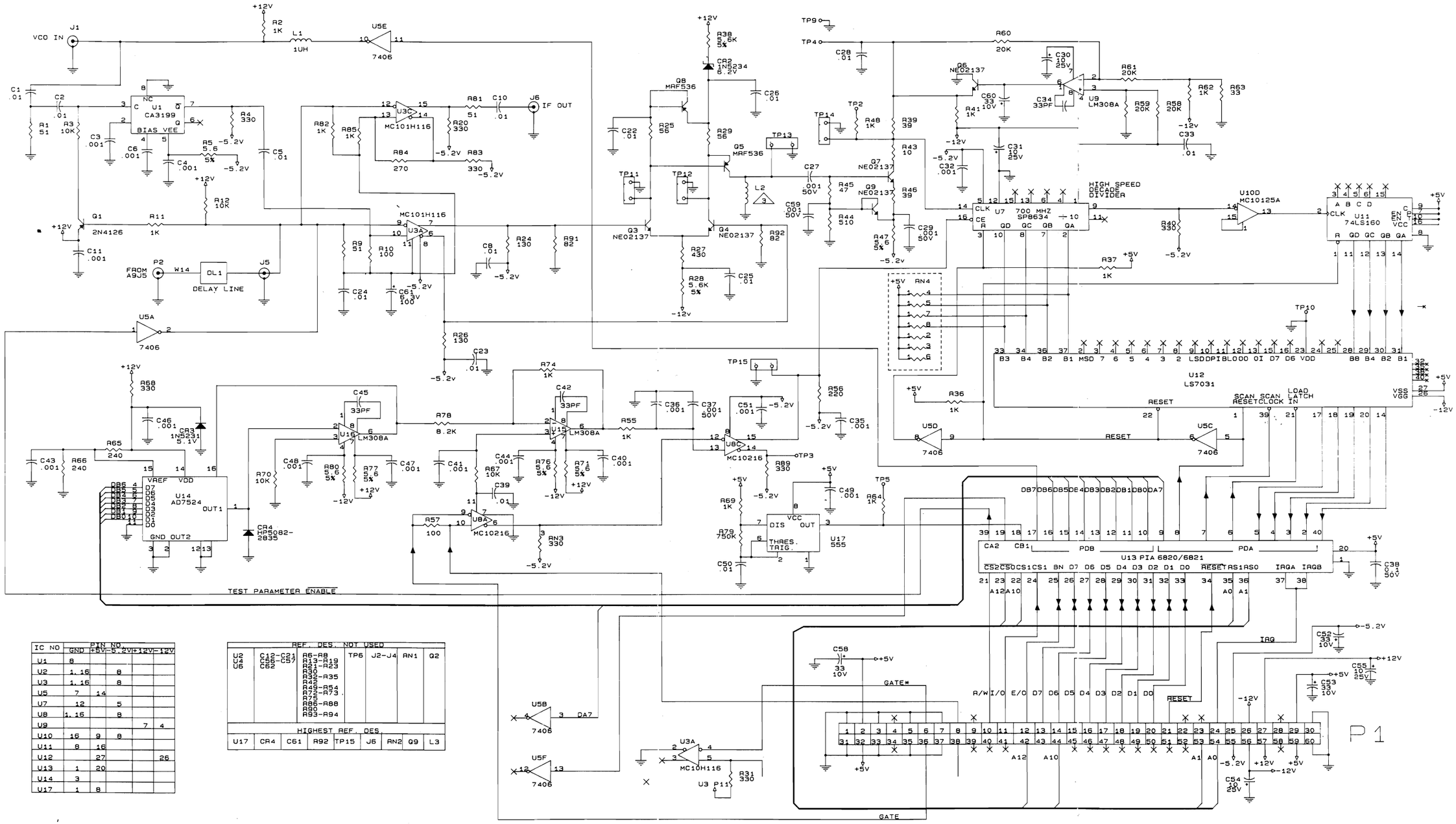


Figure 10-15. Count Chain (A6) Component Locator.



IC NO	PIN NO. GND	+5V	-5.2V	+12V	-12V
U1	8				
U2	1, 16		8		
U3	1, 16		8		
U5	7	14			
U7	12		5		
U8	1, 16		8		
U9				7	4
U10	16	9	8		
U11	8	16			
U12		27			26
U13	1	20			
U14	3				
U17	1	8			

REF. DES. NOT USED							
U2 U4 U6	C12-C21 C56-C57 C62	R6-R8 R13-R19 R21-R23 R30 R32-R35 R42 R45-R54 R72-R73 R75 R86-R88 R90 R93-R94	TP6	J2-J4	RN1	Q2	
HIGHEST REF. DES.							
U17	CR4	C61	R92	TP15	J6	RN2	Q9	L3

3 LS IS PART OF PC BOARD.
2 ALL CAPACITORS ARE IN MICROFARADS, 100V.
1 ALL RESISTORS ARE IN OHMS 1/4W, 2%
NOTES: UNLESS OTHERWISE SPECIFIED

5500404-01 E

Figure 10-16. Count Chain (A6) Schematic Diagram.

A7
GATE GENERATOR
(2020217-04)

The gate generator assembly generates the gate signal for frequency measurement and for pulse width and pulse period measurements. In the frequency measurement mode, it controls the time interval needed for the required resolution.

The gate generator assembly consists of the following functional blocks:

- Reject gate circuit
- Loss-of-lock detector
- Parameter gate processor
- Frequency gate processor
- Accumulator
- 10 MHz reference oscillator
- 80 MHz phase lock loop (PLL) source

Control and timing of the gate generator board (A7) signals are managed by the microprocessor through a peripheral interface adapter (PIA).

SIGNAL PATH

The detected IF signal (digital signal, ECL levels) input from the signal conditioner (A9) is applied to the reject gate circuit, which partially or completely supressed the gate if: (1) detected IF signal (active ECL high) arrives in less than 200 ns from the trailing edge of the preceding detected IF signal, thus eliminating the possibility of triggering on input noise, or (2) it is disabled by an active inhibit signal.

The output from the reject gate circuit (gate enable) is distributed to the parameter gate processor and the frequency gate processor. The parameter gate processor provides two pulses that indicate the beginning and the end of the signal respectively. The frequency gate processor shortens the leading edge of the gate signal so the gate signal by 30 ns so the gate signal input to the count chain board occurs in the middle of the IF pulse.

Both outputs from the reject gate circuit are applied to the accumulator. During the frequency measurement mode, the gate signal is sampled by an 80 MHz clock, so that accumulator output gate width is a multiple of 12.5 ns time intervals. The output is divided between the count chain board and the accumulator. The accumulator counts the clock for one or more gate periods and terminates the current measurement cycle whenever it accumulates the total gate time necessary to achieve the requested resolution.

In the parameter measurement mode, the accumulator output equals the width or the period of the input pulse. This output is applied only to the count chain board. In this mode, the clock is shut off and the accumulator is disconnected.

The 80 MHz clock is provided by a phase-locked loop source that receives a 10 MHz reference signal from the 10 MHz reference clock. This 10 MHz clock can be the internal crystal oscillator or an external source provided through the rear panel. The 10 MHz reference signal is also applied to the Band 2 converter module.

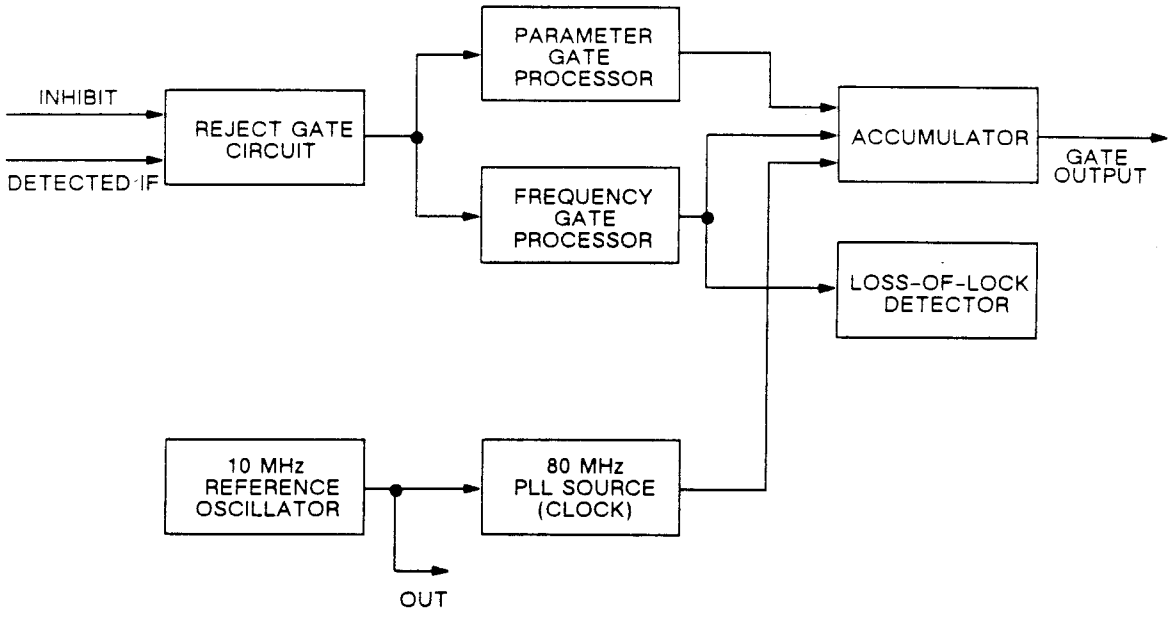


Figure 10-17. Gate Generator Block Diagram.

REJECT GATE CIRCUIT

This circuit block inhibits the gate when:

1. The signal is less than 200 ns from the trailing edge of the preceding gate (in which case it may be noise or high PRF that is out of specification and should, therefore, be eliminated). This inhibit is implemented by U16, a D flip-flop. U16 pin 7 is driven high by R36 and R35. When the gate signal ends, the negative transition triggers the flip-flop, forcing the Q output, pin 2, high and disabling U9B at pin 11. Capacitor C24 is charged to a high level through R39; when it reaches the appropriate voltage, after approximately 200 ns it resets the flip-flop and enables U9B.

2. An inhibit signal is received from the rear panel.

LOSS-OF-LOCK DETECTOR

This circuit indicates to the microprocessor whether or not there is a signal. The circuit consists of a set-reset flip-flop (U16B). The microprocessor resets the flip-flop through the PIA pin 16, and after a period of time set by the MIN PRF function, checks to ascertain whether any gate signal has set it. If the flip-flop is not set, the microprocessor assumes the signal has been removed and initiates the converter search procedure.

PARAMETER GATE PROCESSOR

The parameter gate processor circuit provides the count chain board with a gate signal equal in width to the pulse width or the pulse period of the input signal. The parameter gate processor gets its input from the reject gate circuit and shares its output with U11A and U10A

in the gate frequency processor circuit. During parameter measurement, gate flip-flop U11A is used as a set-reset flip-flop; during frequency measurement, it is used as a D flip-flop.

The parameter gate processor is enabled only when pulse width or pulse period measurement is selected. The gate signal is input at the junction of U3B pin 6 and U6A pin 6. U3B is an inverter used during pulse width measurement and enabled at pin 7 when the pulse width line is low. U6A functions as a divide-by-two counter (pin 3 is connected to pin 7). It is a positive edge triggered flip-flop that is enabled at pin 4 (reset) when the pulse-period line is low. U6 divides the frequency of the pulse-train by two, forming a square wave signal whose width is equal to the original gate period. The signal at U3D pin 13 is a pulse whose width is equal to either the pulse width or the pulse period, depending on the selected parameter.

The circuit consisting of U7, U3D, U12B, and U12D is a pulse-forming network. It has input at U3B pin 13 and puts out two very short pulses on two different lines. The pulse output at U12B pin 3 marks the beginning of the pulse or period gate signal; the pulse output at U12D pin 15 points at the termination of the pulse or period gate. These signals serve as the set-reset signals to the input of U11A.

Before the measurement cycle begins, the flip-flop U11 must be reset by the board reset signal provided by U18 pin 10 through U23A, U2B, and U12A. The 80 MHz clock at U11A pin 9 that exists during the frequency mode is inhibited by a high logic signal at U4A pin 5.

Since U11A is in the set state, only a short pulse on the reset line (pointing to the leading edge of the pulse) at pin 4 switches its state, and the next short pulse on the set line, pin 5, returns it to the original state. The negative-going change on U11A pin 2 and U11B pin 11 causes U11B to switch states and terminate this measurement cycle by placing a high logic signal at U3D pin 12. The gate signal at U11A pin 3 is applied to the count chain board through U10A and pin 6 and 36 at the edge connector.

FREQUENCY GATE PROCESSOR

The frequency gate processor block is enabled when the pulse width and pulse period lines are both low. the frequency gate processor receives a gate signal, an inverted pulse, from U9B pin 7 in the reject gate circuit. It then generates a gate the width of which is a multiple of 12.5 ns time intervals. This gate is shortened by approximately 30 ns from the original gate in the following manner: a capacitor to ground, C14, slows the fall time of the inverted gate signal without greatly affecting the rise time.

The signal is squared up again by a Schmitt trigger consisting of U15, R26, and R27. After passing through U9A, which is enabled by its other input being low, the gate signal reaches pin 7 of the gate flip-flop U11A. This is a fast ECL D flip-flop. This clock, at pin 9, comes from the 80 MHz PLL source through U4A, provided the enable signal at pin 5 is low.

When the gate signal reaches the input of the gate flip-flop, the gate flip-flop is triggered by the next 80 MHz clock pulse. When the gate period ends or when the accumulator is full (U9C pin 14 is high), the next 80 MHz clock pulse turns the gate flip-flop back to the preceding state. The gate flip-flop outputs the gate signal to the accumulator, at U11B pin 11, and to the count chain board on differential lines through U10A to pins 6 and 36 of the edge connector. The reset signal from U18 pin 10 is applied at U11A pin 5 from U12A Pin 2 and causes the gate flip-flop U11A to be set at the beginning of the measurement cycle.

ACCUMULATOR

The accumulator is a high-speed binary upcounter that counts the 80 MHz clock during the measurement cycle and stops count when its state is equal to a preset value. This value is one of five predefined maximum clock counts that the 80 MHz clock translates to total gate time of 0.1 μs, 1 μs, 10 μs, 100 μs, or 1 ms.

The accumulator input comes from the 80 MHz clock at U11A pin 9. It has two outputs. The first, at U18 pin 12, tells the microprocessor that the measurement is over. The second output, at U9C pin 14, is an inhibit signal to the gate flip-flop U11A pin 7 (wire-ORed with U9B), which delivers the gate signal. the accumulator counts only when U11B pin 13 (the clock enable) is low. The control lines of the accumulator are the reset and gate time lines.

There are five phases of Accumulator operation:

1. **Premeasurement.** No gate signal is present. Gate flip-flop input D (U11A pin 7) is high. As a result, its Q output is high and the accumulator is disabled.

2. **Beginning of the gate.** Input D of the gate flip-flop changes state to low. The next 80 MHz clock signal triggers the gate flip-flop, forcing the Q output to change to low level. This enables the accumulator, but because of the inherent delay of this IC, the accumulator does not count this clock pulse.

3. **Measurement.** The accumulator begins count on the next clock pulse and continues until it is disabled again at the enable input.

4. **End of the gate.** The gate flip-flop input D changes state to high. On the next clock pulse, its Q output follows the input and disables the accumulator. Because of the inherent delay of this IC, the accumulator counts this clock pulse.

During pulse measurement, phases 2, 3, and 4 repeat until the sum of the total gate time approaches that of the preset gate time.

5. **End of Measurement.** After the nth count, the accumulator inhibit output (U9C pin 14) issues a high signal to the wired-OR junction of the D input of the gate flip-flop. On the next clock pulse, the gate flip-flop outputs a change of state (in the pulse mode, the change occurs at the middle of the current gate), preventing continuation of measurement.

The accumulator comprises a divide-by-eight ECL counter (U11B, U5, and U6B) followed by four TTL-level decade counters (U19 and U21). The count capacity of this group is 80,000 clock pulses, which at an 80 MHz (12.5 ns) clock rate totals 1 ms. The last three decade counters (U19A, U21A, and U21B) may be removed from the string to permit the shorter gate times mentioned previously. This is done by putting a high level on the set line of the decade counters (pin 4 or 12). In addition, a divide-by-four counter (U22), which may be switched into or out of the chain, is included between the binary and the decade counter. The divide-by-four circuit is included when the counter is operating in Bands 1 or 3 to increase the gate time by a factor of four. The output of those bands is prescaled by four, so the gate time must be extended to cause the counter to read the input frequency directly. This function is controlled by pin 7 of the PIA. In Band 2, the divide-by-four circuit is disabled, and gate U23B provides a path for the input signal around the stage.

A coincidence detector (U20) produces a low output when all the decade counters are in state 9 and the divide-by-four is in state 3. A second coincidence detector (U4B) produces a high

level output when U5A, U5B, and U6B are in the 1 position. A third coincidence detector (U9C) produces the accumulator inhibit signal by using the outputs of the two previous coincidence detectors, U20 and U4B, to produce a coincidence after n clock pulses. A fourth coincidence detector (U10B) sends the end-of-measurement message to the PIA through pin 7 and prevents any further counting by putting a high level on the set pin 12 of U11B.

It is important to remember that the gate signal itself consists of n+1 clock pulses, since the first pulse is not taken into account by the accumulator.

To repeat the measurement, a reset signal is sent by the PIA. The reset causes the coincidence detector U9C to release the inhibit. Since this occurs last in the series of accumulator counting operations, invalid data is not generated.

10 MHz REFERENCE OSCILLATOR

The 10 MHz reference oscillator is the time base for the counter. Its reference is either an internal 10 MHz TCXO or an external reference source connected to rear panel connector J3. The required reference source (internal or external) is selected at the front panel. The selection is input from PIA U18 pin 2 to pins 5 and 8 of dual comparator U25. A low TTL logic level from U18 means the TCXO input is selected. U25 squares the sine wave input and delivers TTL output levels through U24A as a frequency reference to two phase-locked loop (PLL) circuits: to pin 1 of U8 (the 80 MHz PLL), and through connector J4 to the converter control board. When an internal reference source is chosen, this signal is also available at the rear panel through U23B, Q6, and J3.

When an external reference is used, pin 4 of U25 is high and causes Q6 to be off, so that the external 10 MHz signal reaches U25 pin 12 through J3, a two-way (input-output) connector.

80 MHz PHASE-LOCKED LOOP

The PLL circuit provides an accurate 80 MHz clock for the accumulator circuit. The voltage controlled oscillator (VCO) consists of U1 and the varactor CR1. The VCO delivers its output to a divide-by-18 divider consisting of U13 and U14. This 10 MHz ECL output is ac coupled through C11 and translated to TTL levels by Q5. The phase detector U8 compares this signal (applied to pin 3) with the 10 MHz reference (pin 1) and generates a dc signal proportional to the phase difference. Deviation from 80 MHz causes voltage change at the VCO input in a direction that will return the frequency to 80 MHz. The output is applied to the accumulator circuit via a switch during frequency measurement only. The switch consists of pin 4 of U4A, which serves as an input, pin 3 of U4A, which acts as an output, and pin 5 of U4A, which is the control. In parameter measurement mode, pin 5 of U4A is high and shuts off the switch.

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A7 GATE GENERATOR 2020217-04 Rev. A

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		NOT USED					
C2		CAP,SMD,CER,NPO	.001µF	5%	50V	2100050-00	1
C3		NOT USED					
C4		CAP,DISC,CER,X7R	.1µF	10%	50V	2150028-00	9
C5	C4						
C6		CAP,MICA	560PF	5%	500V	2250036-00	1
C7		CAP,TANTALUM	33µF		10V	2300015-00	5
C8	C4						
C9		CAP,ML CER	.01µF	10%	100V	2150014-00	11
C10	C4						
C11	C4						
C12		NOT USED					
C13	C7						
C14		CAP,CER SEE NOTE 1	220PF	10%	100V	2150047-00	1
C15	C9						
C16		NOT USED					
C17	C9						
C18	C9						
C19	C4						
C20	C9						
C21	C7						
C22	C9						
C23	C4						
C24		CAP,MICA	100PF	5%	500V	2260034-00	1
C25	C9						
C26	C9						
C27	C7						
C28		CAP,TANTALUM	10µF	20%	25V	2300029-00	1
C29	C7						
C30	C4						
C31	C4						
C32	C9						
C33	C9						
C34	C9						
C35		CAP,SMD,CER,NPO	220PF	10%	50V	2100107-00	1
C36		CAP,SMD,CER,NPO	390PF	10%	50V	2100106-00	1
CR1		DIODE,MV209,VARIABLE CAP				2710012-00	1
J1		NOT USED					
J2		NOT USED					
J3		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	2
J4	J3						
L1		INDUCTOR,.1µH				3510001-00	1
L2		INDUCTOR,1.0µH				3510003-00	1
Q1		NOT USED					
Q2		NOT USED					
Q3		NOT USED					
Q4		NOT USED					
Q5		XSTR,2N4124,NPN,GP				4704124-00	1
Q6		XSTR,2N4126,PNP,GP				4704126-00	1
R1		NOT USED					
R2		NOT USED					
R3		NOT USED					
R4		RES,MF	1K	1/4W	2%	4130102-00	8
R5		RES,MF	36K	1/4W	2%	4130363-00	1

NOTE 1 - SAT AS FOLLOWS: 100PF MIN-470PF MAX

A7 GATE GENERATOR (Continued) 2020217-04 Rev. A

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R6		RES,MF	150	1/4W	2%	4130151-00	1
R7		RES,CC	2.7	1/4W	5%	4010279-00	3
R8		RES,MF	300	1/4W	2%	4130301-00	3
R9		RES,MF	680	1/4W	2%	4130681-00	1
R10		RES,MF	4.3	1/4W	2%	4130432-00	2
R11		RES,MF	510	1/4W	2%	4130511-00	1
R12		RES,MF	330	1/4W	2%	4130331-00	11
R13	R7						
R14	R4						
R15		NOT USED					
R16		NOT USED					
R17	R8						
R18		NOT USED					
R19		NOT USED					
R20		NOT USED					
R21		NOT USED					
R22		NOT USED					
R23		NOT USED					
R24		RES,MF	2K	1/4W	2%	4130202-00	1
R25	R12						
R26		RES,MF	390	1/4W	2%	4130391-00	2
R27	R26						
R28	R12						
R29	R12						
R30		RES,MF	100	1/4W	2%	4130101-00	1
R31	R12						
R32		NOT USED					
R33		NOT USED					
R34		NOT USED					
R35	R10						
R36		RES,MF	820	1/4W	2%	4130821-00	1
R37	R12						
R38	R12						
R39	R4						
R40	R7						
R41		RES,MF	1.8K	1/8W	2%	4130182-00	2
R42		RES,MF	1.2K	1/4W	2%	4130122-00	1
R43	R41						
R44	R12						
R45		RES,MF	10K	1/4W	2%	4130103-00	3
R46	R45						
R47	R45						
R48	R12						
R49	R8						
R50		RES,MF	30	1/8W	2%	4130300-00	1
R51	R4						
R52	R4						
R53		RES,CC	5.1	1/4W	5%	4010519-00	2
R54	R4						
R55	R53						
R56	R4						
R57	R12						
R58	R12						
R59	R4						
R60		RES,SMD	39.2	1/8W	1%	4220054-00	1
RN1		RES,NTWK	7X330	.8W	2%	4170010-00	3
RN2	RN1						
RN3		RES,NTWK	9X330	.3W	2%	4170011-00	2
RN4	RN1						
RN5	RN3						
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	5
TP2	TP1						

A7 GATE GENERATOR (Continued) 2020217-04 Rev. A

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
TP3	TP1			
TP4	TP1			
TP5	TP1			
U1		IC,MC1648,OSC,VOLTAGE CONTROLLED	3011648-00	1
U2		IC,10124,ECL 10K,TRANSLATOR	3110124-00	1
U3		IC,10102,ECL 10K,2-INP NORS	3110102-00	2
U4		IC,10105,ECL 10K,OR/NOR GATES	3110105-00	3
U5		IC,10131,ECL 10K,M-S FF	3110131-00	5
U6	U5			
U7		IC,10107,ECL 10K,2-IN EXCL OR/NOR	3110107-00	1
U8		IC,MC4044,PHASE FREQ DET	3014044-00	1
U9	U4			
U10	U4			
U11	U5			
U12	U3			
U13	U5			
U14		IC,DGTL,D FF	3110231-01	1
U15		IC,10116,ECL 10K,LINE RCVRS	3110116-00	1
U16	U5			
U17		IC,10125,ECL 10K,TRANSLATORS	3110125-00	1
U18		IC,6820,PERIPHERAL INTFC ADAPTER	3086820-00	1
U19		IC,74LS490	3084490-00	2
U20		IC,74S133	3070019-00	1
U21	U19			
U22		IC,74LS76A	3087476-00	1
U23		IC,74LS11	3087411-00	1
U24		IC,74ACT00PC	3110011-00	1
U25		IC,521,DUAL DIFF COMPARATOR	3050521-00	1
XU1		NOT USED		
XU2		NOT USED		
XU3		NOT USED		
XU4		NOT USED		
XU5		NOT USED		
XU6		NOT USED		
XU7		NOT USED		
XU8		NOT USED		
XU9		NOT USED		
XU10		NOT USED		
XU11		NOT USED		
XU12		NOT USED		
XU13		NOT USED		
XU14		NOT USED		
XU15		NOT USED		
XU16		NOT USED		
XU17		NOT USED		
XU18		NOT USED		
XU19		NOT USED		
XU20		NOT USED		
XU21		CONN,IC PIN(MINISERT)	2620054-00	16
Y1		OSC,TCXO	2030002-00	1
HARDWARE USED IN THIS ASSEMBLY				
		TUBING,TEFLON,22 AWG	5480008-00	0.4
		BUS BAR,MINI,3 LAYER	5000226-00	1
		HANDLE,PCB	5230001-00	2
		PIN,ROLL,3/32 DIA 1/4 LG	5110008-00	2
		PCB SCHEMATIC DIAGRAM	5500217-01 B	REF.

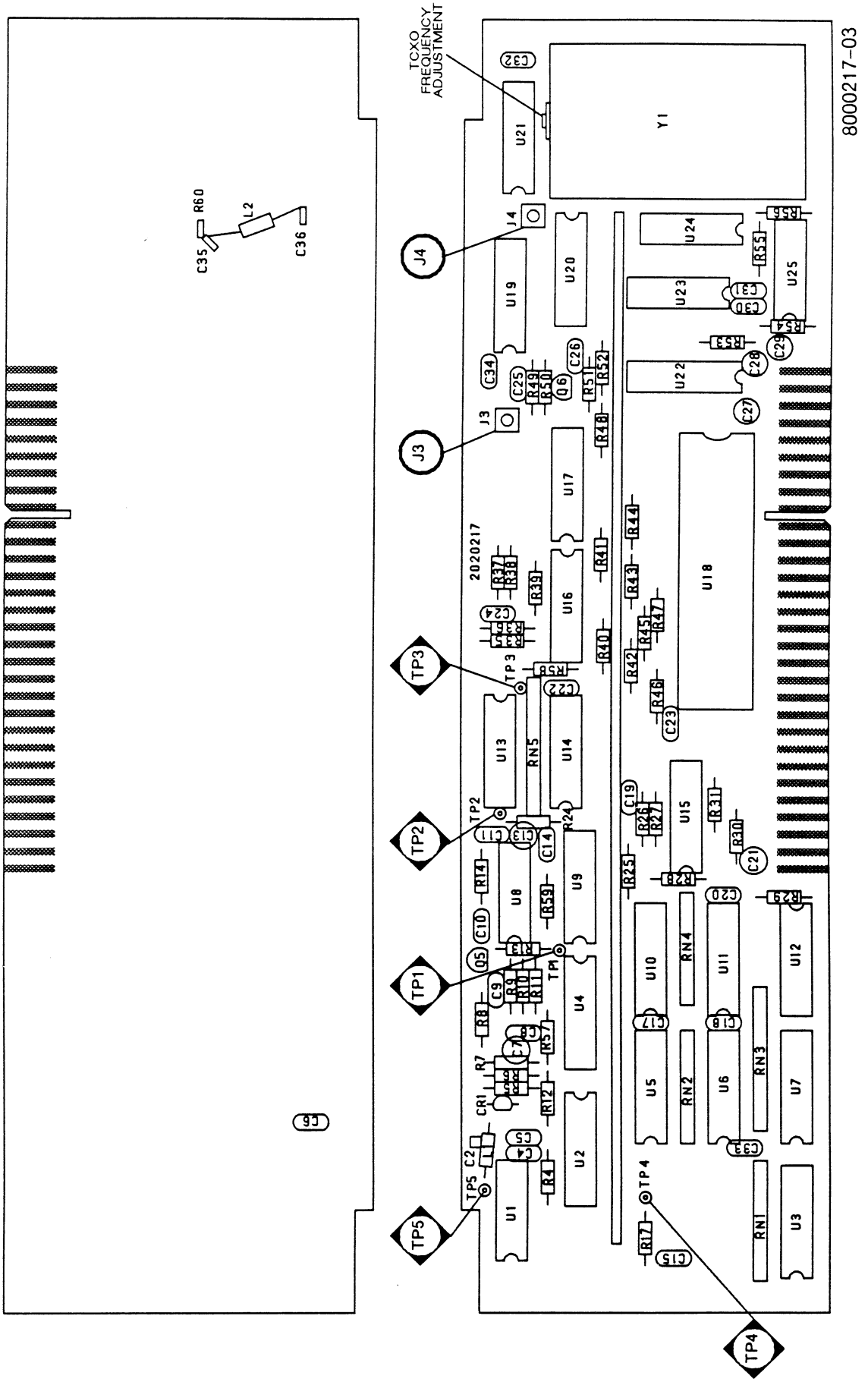
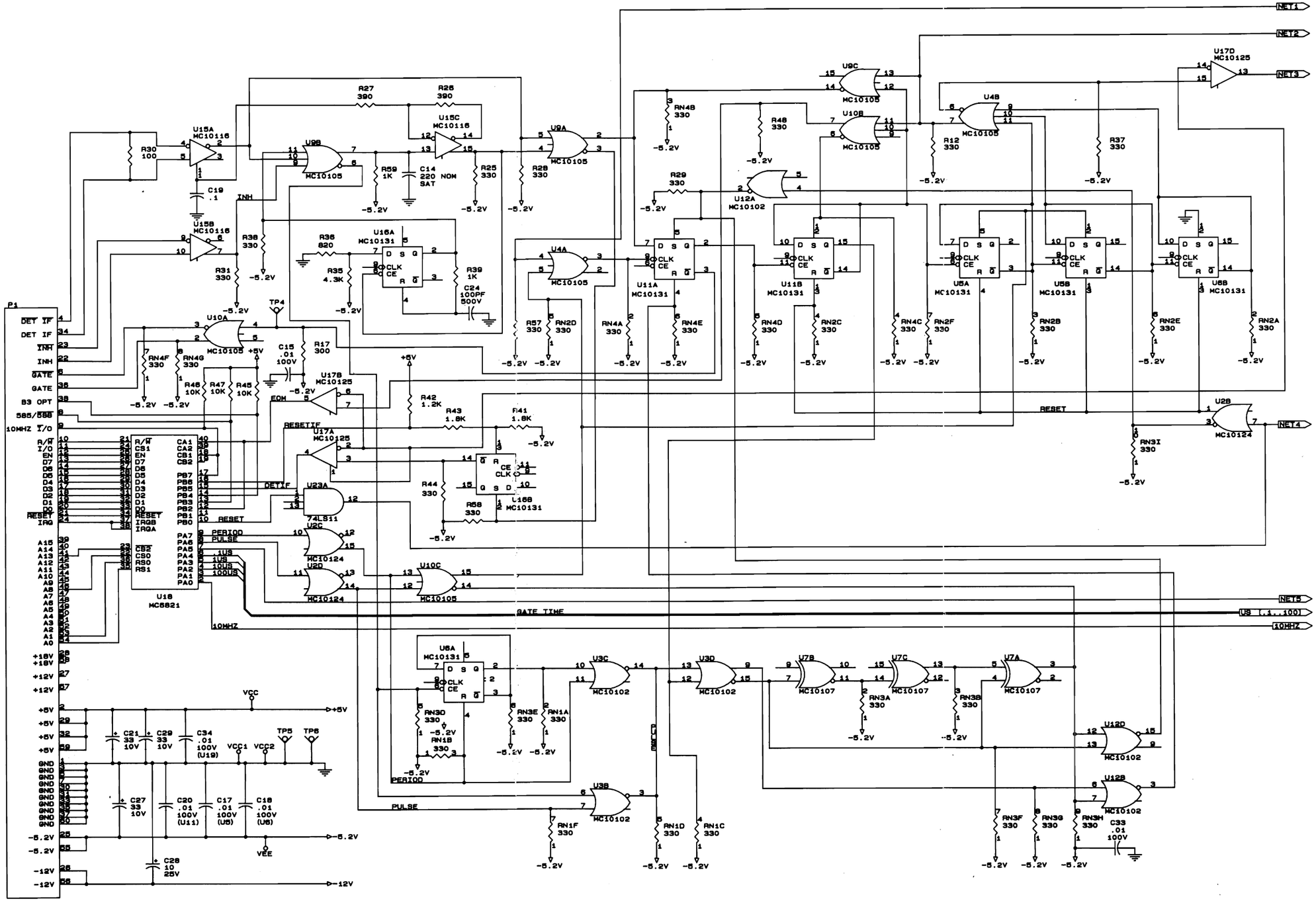


Figure 10-18. Gate Generator (A7) Component Locator.



2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/4W, 2%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500217-01 B

Figure 10-19. Gate Generator (A7) Schematic Diagram. (Sheet 1 of 2)

IC NO	IC TYPE	PIN NUMBERS		
		GND	+5V	-5.2V
U1	MC1648	1, 14		
U2	MC10124	16	9	8
U3, U12	MC10102	1, 16		8
U4, U9, U10	MC10105	1, 16		8
U5, U6, U11, U16	MC10131	1, 16		8
U7	MC10107	1, 16		8
U8	MC4044	7		
U13	MC10131	1, 16		
U14	MC10231	1, 16		
U15	MC10116	1, 16		8
U17	MC10125	16	9	8
U18	MC6820	1	20	
U19, U21	74LS490	8	16	
U20	74S133	8	16	
U22	74LS76	13	5	
U23	74LS11	7	14	
U24	74ACT00	7		
U25	NE521	7		

REFERENCE DESIGNATORS	
LAST USED	NOT USED
R60	R1, R2, R3, R15, R16, R18, R19, R20, R21, R22, R23, R32, R33, R34
C36	C1, C3, C12, C16
CR1	
L2	
Y1	
Q6	Q1, Q2, Q3, Q4
RN5	
U25	
TP6	
J5	J1, J2, J5

5500217-01 B

Figure 10-19. Gate Generator (A7) Schematic Diagram (Sheet 2 of 2)

A8
GATE CONTROL
(2020405-02)

Gate Control Assembly A8 provides three basic functions: it buffers the gate signal, it buffers the detected IF signal from the rear panel, and it provides the inhibit enable/disable control. The gate signal buffer consists of line receiver U1C and differential amplifier Q2-Q1, which provides a 0 to -1 V signal into 50 ohms. The detected IF signal buffer consists of line receiver U1A and differential amplifier Q3-Q4 that provides a 0 to -1 V signal into 50 ohms. Line receiver U1B enables or disables the inhibit input from the rear panel. The control line for the line receiver is provided by PAL U2, which is used as a decoder.

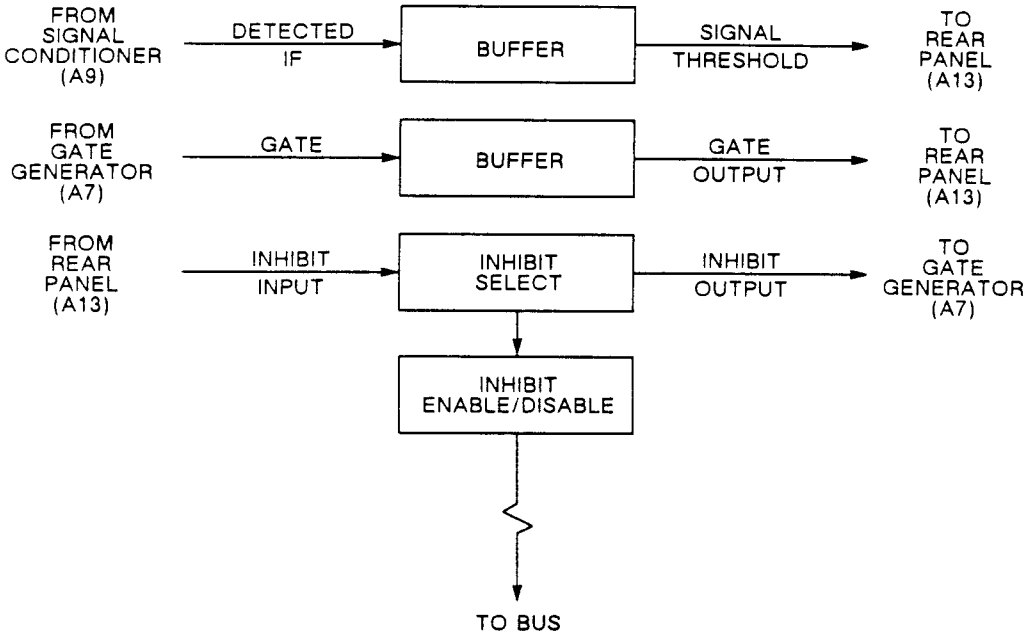


Figure 10-20. Gate Control Block Diagram.

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A8 GATE CONTROL

2020405-02 Rev. C

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,SMD,CER,X7R	.01µF	10%	50V	2100040-00	4
C2	C1						
C3	C1						
C4		CAP,SMD,TANT	10µF	10%	25V	2100043-00	2
C5	C4						
C6	C1						
CR1		DIODE,SMD,HSMS-2822				2740001-00	1
J1		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	3
J2	J1						
J3	J1						
Q1		XSTR,SMD,MMBT2369,NPN,SWITCHING				4730024-00	4
Q2	Q1						
Q3	Q1						
Q4	Q1						
R1		RES,SMD	150	1/8W	1%	4231500-00	4
R2		RES,SMD	51.1	1/8W	1%	4235119-00	2
R3		RES,SMD	332	1/8W	1%	4233320-00	6
R4	R3						
R5	R1						
R6		RES,SMD	162	1/8W	1%	4231620-00	2
R7		RES,SMD	100	1/8W	1%	4231000-00	2
R8	R6						
R9		RES,SMD	274	1/8W	1%	4232740-00	2
R10	R9						
R11	R2						
R12	R1						
R13	R1						
R14	R3						
R15	R3						
R16	R3						
R17	R3						
R18		NOT USED					
R19	R7						
R20		RES,SMD	511	1/8W	1%	4235110-00	1
R21		RES,SMD	2.21K	1/8W	1%	4232211-00	2
R22		RES,SMD	1.10K	1/8W	1%	4231101-00	1
R23	R21						
U1		IC,SMD,MC10H116				3170042-00	1
U2		PAL,PRGM				2070087-00	1
HARDWARE USED IN THIS ASSEMBLY							
		HANDLE,PCB				5230001-00	2
		PIN,ROLL,3/32 DIA 1/4 LG				5110008-00	2
		PCB SCHEMATIC DIAGRAM				5500405-02 C	REF.

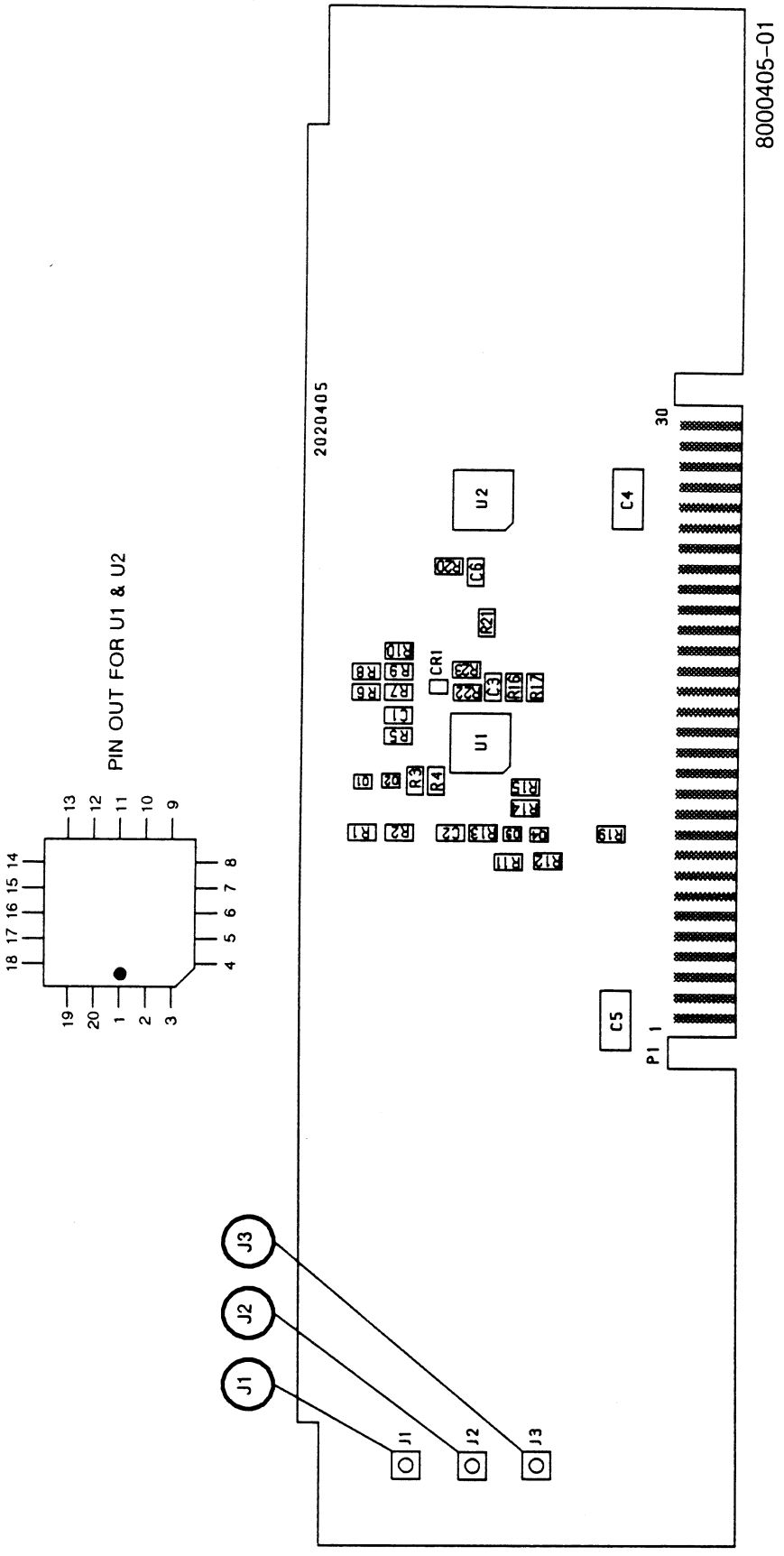
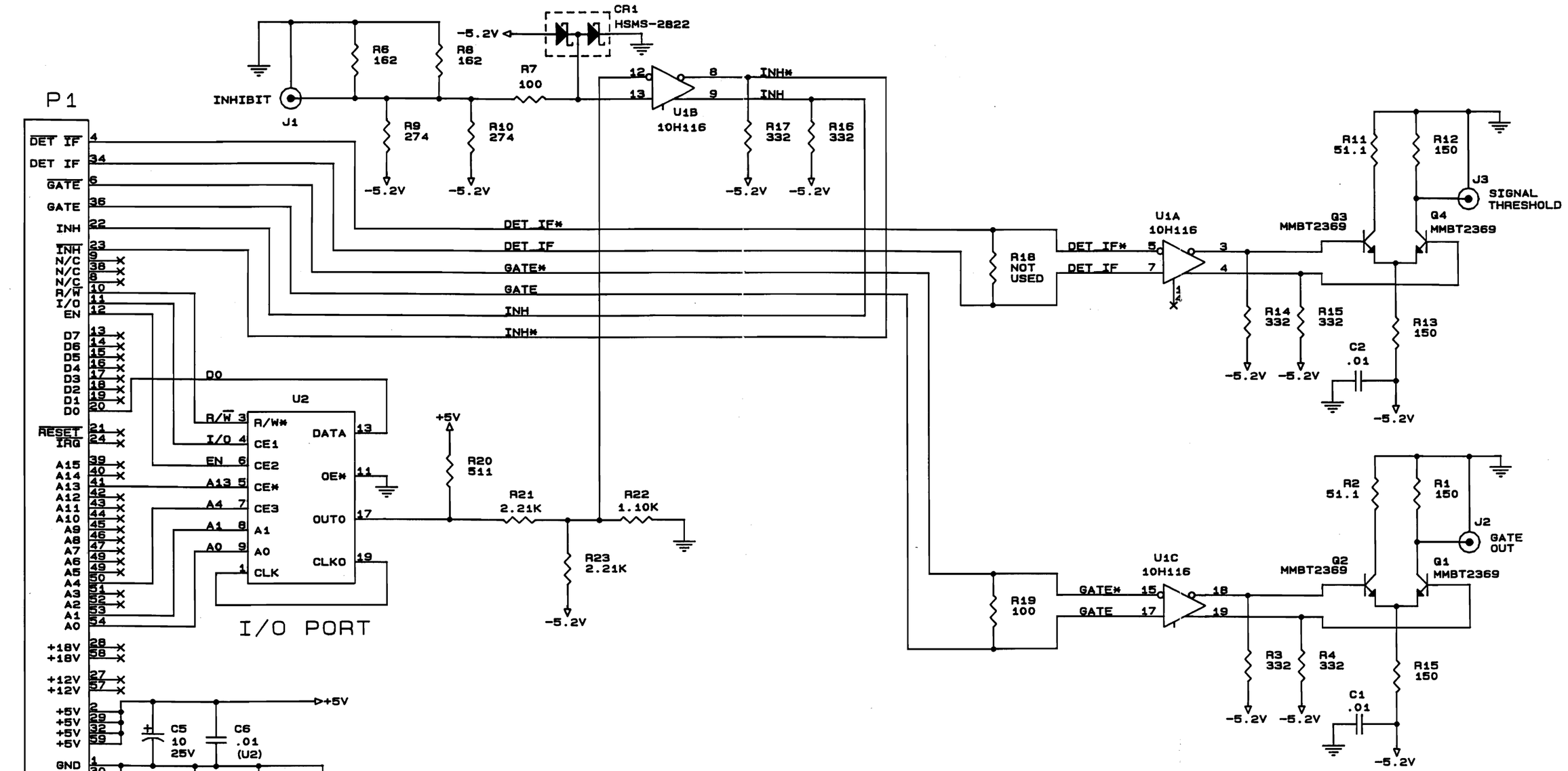


Figure 10-21. Gate Control (A8) Component Locator.



LAST USED	NOT USED
C6	
CR1	
R23	R5
U2	
P1	
J3	
Q4	

IC NO.	IC PIN NO.		
	+5V	GND	-5.2V
U1		2, 20	10
U2	20	10	

5500405-02 C

2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPS. ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W, 1%.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 10-22. Gate Control (A8) Schematic Diagram

A9
SIGNAL CONDITIONER
(2020395-10)

Signal conditioner PCB assembly A9 processes signals from all bands before they are applied to count chain PCB assembly A7 to be counted. When the counter finds a signal of appropriate amplitude, the signal conditioner generates a threshold signal (ECL level) that lasts for the duration of the input signal. This threshold signal is used by gate generator PCB assembly A6 to generate the gate needed and to measure pulse parameters. The signal conditioner determines the amplitude of the video signal generated in Band 2 converter assembly A10. This signal is proportional to the RF level applied to the Band 2 input. Figure 10-23 shows the following:

- Video amplitude determination
- Inhibit signal
- Signal path
  Band 0
  Band 1
  Band 2
  Band 3
- Output processing

VIDEO AMPLITUDE DETERMINATION

The video amplitude determination circuit converts the analog video signals into digital signals for use by the microprocessor. The video signal at J6 is first routed through a 15 MHz lowpass filter (C80, L10, C81) to filter out any unwanted high frequency noise. The signal is then applied to a flash A/D converter circuit (U17 through U20) consisting of eight comparators arranged in two sets of four comparators each. The reference levels for these comparators are set by resistive voltage dividers spaced 5 dB apart and are driven by a DAC (U14) through a X2.5 amplifier (U16). The 16 bit DAC is driven by the microprocessor through a PAL (U22) that provides the control signals for the DAC. The outputs of the A/D converters are applied to two 4 bit latches (U23 and U24). These latches hold the A/D output data until they are reset by the microprocessor through U26 and U27A. The latch outputs are then applied to an 8 bit parallel-to-serial converter (U25). The microprocessor reads this information by shifting one bit at a time through converter U25 and buffer U28A.

INHIBIT SIGNAL

The inhibit input signal from gate control PCB assembly A8 is applied to ECL-to-TTL converter U29A. The converter output enables or disables the eight comparators (U17 through U20), depending on the state of the inhibit signal.

SIGNAL PATH

Signals from Bands 0 through 3 are processed in four basic steps. First, the amplitude of the signal is set to a desired level; second, the signal is routed through a PIN diode switch into a common node for Bands 1, 2, and 3. These PIN diode switches select the signal for the desired band. Third, the signal is applied to a threshold circuit to assure proper signal level, and, fourth, the proper output is chosen for the desired band, i.e., normal or divide or four.

BAND 0

Band 0 (100 Hz – 250 MHz CW only) is a direct count band, i.e., no prescaling is required. The input signals at J8 are first routed through a limiter (CR19) for protection from high amplitude signals and then through a power amplifier/impedance converter (Q1, Q2) to provide proper drive for 50 ohm input of amplifier U31. The signal is then amplified in a 25 to 30 dB amplifier (U31) whose output is then routed through output select circuit U8 and U7 and sent (via J5) to Count Chain Assembly A6 to be counted.

BAND 1

In this band, the signal is first applied to a 6 dB T-pad (R90 through R92) to provide proper termination for isolation. The signal is then passed through a single pole, 60 MHz low pass filter (C14 and L5) to provide low end cutoff. The next stage consists of 12 dB amplifier U1 followed by a PIN diode attenuator (CR1, CR2 and CR3) which is driven by DAC U14 through X3 amplifier U15. The attenuator provides a constant power level under various input powers. Attenuator gain is controlled by software. The signal is then routed through a 2-stage amplifier. The first stage (U3) provides about 12 dB gain, and the second stage (U4) provides 20 dB gain which varies with input frequency. The signal is then applied to the output processor through a PIN diode switch consisting of CR6, CR7, and CR9. This switch is only turned on while the counter is in Band 1.

BAND 2

Band 2 is a microwave band; thus, the frequency is first downconverted in Band 2 converter module A10. Only the IF (120 MHz ±25 MHz) is applied to the signal conditioner board at J3. No IF amplification is required at this point since the IF signal is amplified in the Band 2 converter module and sent directly to the output processor via PIN diode switch CR14, CR15, and CR10. This switch is only turned on when the counter is in the Band 2 mode.

OUTPUT PROCESSING CIRCUIT

After appropriate gain adjustments, signals from Band 1, Band 2, and Band 3 are routed to a 12 dB output amplifier (U5). The output of this amplifier is used by three different circuits: First, a signal threshold detector circuit consisting of RF detector CR12, lowpass filter L8 and C35, and comparator U10. This circuit detects when an appropriate level of signal exists. The output of this detector is sent to gate generator PCB assembly A7. Second, an auxiliary IF port circuit from J7 through -14 dB attenuator R37 and R127. Third, a 12 dB amplifier (U6) whose output is sent directly to the output select circuit through inductor L9. This output is also applied to a divide-by-4 IC (U9) and then to the output select circuit. In the Band 2 mode, the divide-by-4 IC is disabled by pulling pin 3 high through CR21 and R89, and normal output is selected via the output select circuit. Since the IF for Bands 1 and 3 is much higher, the divide-by-4 output is selected for these bands.

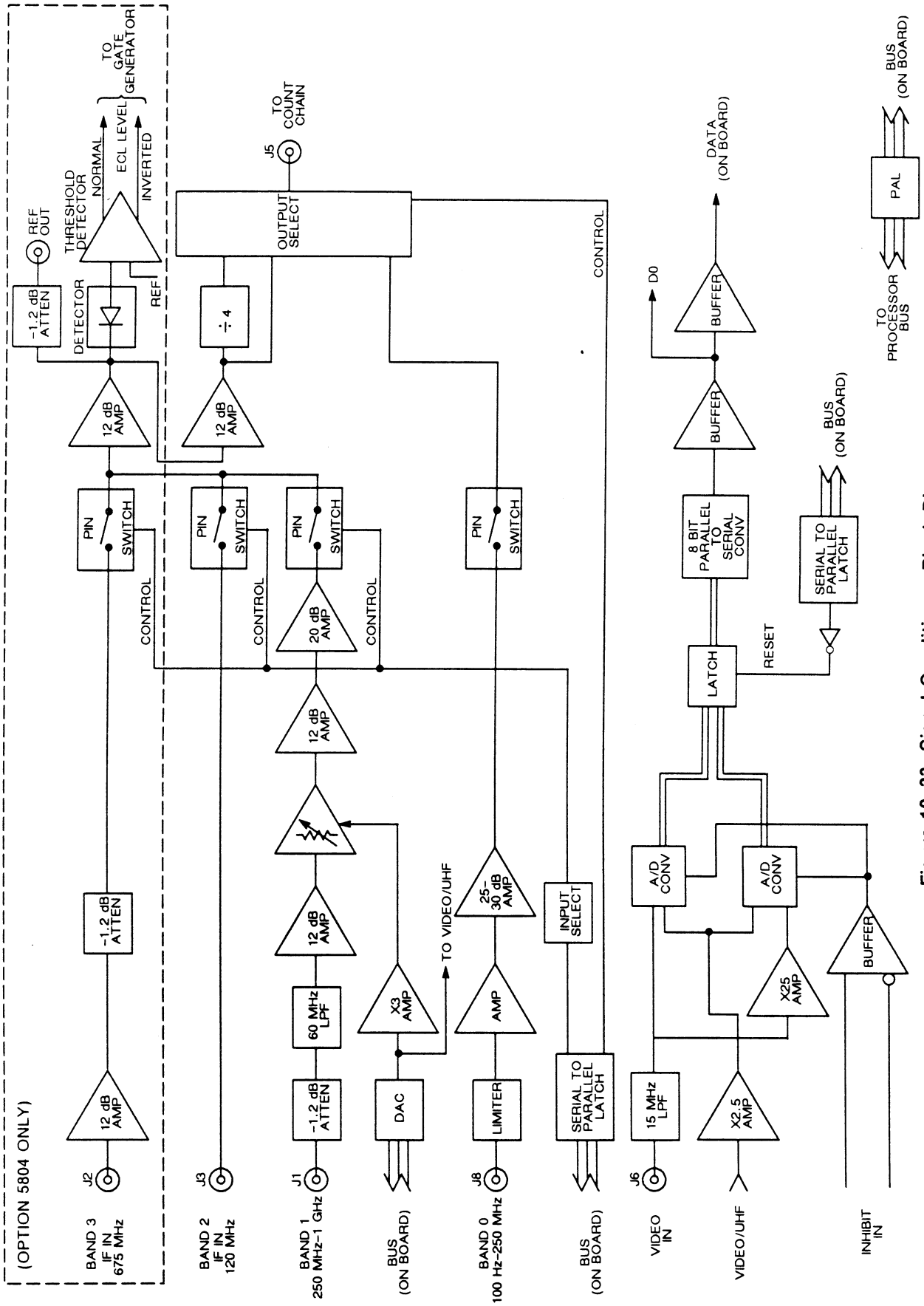


Figure 10-23. Signal Conditioner Block Diagram.

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A9 SIGNAL CONDITIONER 2020395-10 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,SMD,Z5U	.1µF	20%	50V	2100046-00	54
C2		CAP,SMD,CER,NPO	100PF	5%	50V	2100054-00	2
C3	C1						
C4		CAP,SMD,CER,X7R	.001µF	5%	50V	2100037-00	19
C5	C1						
C6	C4						
C7	C1						
C8	C4						
C9	C1						
C10	C1						
C11	C4						
C12	C1						
C13	C4						
C14	C2						
C15		CAP,SMD,CER,NPO	15PF	5%	50V	2100072-00	1
C16		NOT USED					
C17		CAP,SMD,CER,NPO	22PF	5%	50V	2100074-00	1
C18	C4						
C19	C1						
C20	C4						
C21	C1						
C22	C4						
C23	C4						
C24		NOT USED					
C25		CAP,SMD,CER,NPO	10PF	5%	50V	2100032-00	1
C26	C4						
C27	C4						
C28		NOT USED					
C29	C1						
C30	C1						
C31	C1						
C32	C4						
C33	C4						
C34	C1						
C35		CAP,SMD,CER,NPO	68PF	5%	50V	2100077-00	1
C36	C1						
C37	C1						
C38	C1						
C39	C1						
C40	C1						
C41	C1						
C42	C1						
C43	C1						
C44	C1						
C45	C1						
C46	C1						
C47	C1						
C48	C1						
C49	C1						
C50	C4						
C51	C1						
C52	C1						
C53	C1						
C54	C1						
C55	C1						
C56	C1						
C57	C1						

A9 SIGNAL CONDITIONER (Continued) 2020395-10 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C58	C1						
C59	C1						
C60	C1						
C61	C1						
C62	C1						
C63	C1						
C64	C1						
C65	C1						
C66		CAP,SMD,TANT	47µF	20%	6V	2100113-00	4
C67	C1						
C68	C1						
C69	C1						
C70	C4						
C71	C66						
C72	C1						
C73	C1						
C74		CAP,SMD,CER,X7R	.0015µF	10%	50V	2100082-00	1
C75	C4						
C76	C4						
C77	C1						
C78	C1						
C79	C1						
C80		CAP,SMD,CER,NPO	82PF	5%	50V	2100078-00	1
C81		CAP,SMD,CER,NPO	180PF	5%	50V	2100036-00	1
C82	C1						
C83	C1						
C84	C66						
C85		CAP,SMD,TANT	10µF	10%	25V	2100043-00	2
C86	C85						
C87	C66						
C88		CAP,SMD,Z5U	1µF	20%	50V	2100108-00	1
C90	C4						
C91	C4						
C92	C1						
C93	C1						
CR1		DIODE,SMD,HSMP-3830,PIN				2700005-00	12
CR2	CR1						
CR3	CR1						
CR4	CR1						
CR5	CR1						
CR6	CR1						
CR7	CR1						
CR8	CR1						
CR9	CR1						
CR10	CR1						
CR11		NOT USED					
CR12		DIODE,SMD,HSMS-2822				2740001-00	3
CR13		NOT USED					
CR14	CR1						
CR15	CR1						
CR16		NOT USED					
CR17	CR12						
CR18		NOT USED					
CR19		DIODE,SMD,MMBD7000				2740010-00	3
CR20	CR19						
CR21	CR19						
CR22	CR12						

A9 SIGNAL CONDITIONER (Continued) 2020395-10 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
J1		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	7
J2	J1						
J3	J1						
J4		NOT USED					
J5	J1						
J6	J1J7	J1					
J8	J1						
L1		INDUCTOR,SMD,.033µH				3530025-05	6
L2	L1						
L3	L1						
L4	L1						
L5		INDUCTOR,SMD,.082µH				3530025-32	1
L6	L1						
L7	L1						
L8		INDUCTOR,SMD,1.5µH				3530025-15	1
L9		INDUCTOR,SMD,.100µH				3530025-08	1
L10		INDUCTOR,SMD,.470µH				3530025-12	1
L11		INDUCTOR,SMD,2.2µH				3530025-16	1
Q1		XSTR,SMD,MMBF4416,SOT-23				4730014-00	1
Q2		XSTR,SMD,NE02133				4730011-00	1
R1		RES,SMD	100	1/8W	1%	4231000-00	17
R2	R1						
R3		RES,SMD	10	1/8W	1%	4231009-00	11
R4	R1						
R5	R1						
R6	R3						
R7		RES,SMD	1K	1/8W	1%	4231001-00	11
R8		RES,SMD	6.81K	1/8W	1%	4236811-00	3
R9		RES,SMD	68.1	1/8W	1%	4236819-00	6
R10	R9						
R11	R3						
R12	R3						
R13	R1						
R14	R3						
R15	R1						
R16	R1						
R17	R1						
R18	R1						
R19	R8						
R20	R3						
R21	R9						
R22		RES,SMD	15	1/8W	1%	4231509-00	1
R23		RES,SMD	15K	1/8W	1%	4231502-00	1
R24		RES,SMD	2.21K	1/8W	1%	4232211-00	12
R25	R8						
R26	R24						
R27	R24						
R28	R24						
R29	R24						
R30	R24						
R31	R24						
R32	R1						
R33		NOT USED					

A9 SIGNAL CONDITIONER (Continued) 2020395-10 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R34		NOT USED					
R35		RES,SMD	51.1	1/8W	1%	4235119-00	3
R36		NOT USED					
R37		RES,SMD	221	1/8W	1%	4232210-00	5
R38	R37						
R39		NOT USED					
R40	R3						
R41	R1						
R42	R24						
R43		NOT USED					
R44	R24						
R45	R7						
R46	R24						
R47		NOT USED					
R48	R37						
R49		RES,SMD	475	1/8W	1%	4234750-00	6
R50	R49						
R51	R49						
R52		RES,SMD	332	1/8W	1%	4233320-00	4
R53	R49						
R54	R49						
R55	R52						
R56	R24						
R57	R3						
R58		RES,SMD	4.75K	1/8W	1%	4234751-00	1
R59		RES,SMD	47.5	1/8W	1%	4234759-00	4
R60	R37						
R61	R52						
R62	R52						
R63		RES,SMD	10K	1/8W	1%	4231002-00	2
R64	R7						
R65		RES,SMD	4.32K	1/8W	1%	4234321-00	1
R66	R7						
R67	R7						
R68		RES,SMD	2.00K	1/8W	1%	4232001-00	1
R69	R7						
R70		RES,SMD	1.50K	1/8W	1%	4231501-00	3
R71		RES,SMD	3.32K	1/8W	1%	4233321-00	1
R72	R7						
R73		RES,SMD	1.3K	1/8W	1%	4231301-00	1
R74		RES,SMD	750	1/8W	1%	4237500-00	1
R75		RES,SMD	301	1/8W	1%	4233010-00	4
R76	R37						
R77	R70						
R78	R49						
R79	R75						
R80		NOT USED					
R81		RES,SMD	182	1/8W	1%	4231820-00	1
R82		NOT USED					
R83	R1						
R84	R35						
R85		NOT USED					
R86		NOT USED					
R87		NOT USED					
R88	R7						
R89	R63						
R90	R9						

A9 SIGNAL CONDITIONER (Continued) 2020395-10 Rev. E

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R91		RES,SMD	18.2	1/8W	1%	4231829-00	2
R92	R91						
R93		RES,SMD	1 MEG	1/8W	1%	4231004-00	1
R94		RES,SMD	475K	1/8W	1%	4234753-00	1
R95	R59						
R96	R70						
R97	R59						
R98	R7						
R99	R59						
R100		NOT USED					
R101	R1						
R102	R9						
R103	R9						
R104	R3						
R105	R1						
R106	R7						
R107		NOT USED					
R108		NOT USED					
R109		NOT USED					
R110	R1						
R111		NOT USED					
R112	R1						
R113		RES,SMD	2.43K	1/8W	1%	4232431-00	1
R114		RES,SMD	2.74K	1/8W	1%	4232741-00	1
R115	R1						
R116	R24						
R117		RES,SMD	3.01K	1/8W	1%	4233011-00	1
R118	R7						
R119	R3						
R120		NOT USED					
R121	R75						
R122	R3						
R123	R75						
R124		RES,SMD	200	1/8W	1%	4232000-00	2
R125	R124						
R126	R35						
R127		RES,SMD	56.2	1/8W	1%	4235629-00	1
R128		RES,MF	160	1/WW	2%	4130161-00	1
U1		IC,SMD,MSA-0385,MMIC				3170071-00	5
U2	U1						
U3	U1						
U4		IC,SMD,MSA-0885,AMP MMIC				5352005-00	2
U5	U1						
U6	U1						
U7		IC,SMD,10H124,TTL/MECL TRANSLATOR				3170072-00	1
U8		IC,SMD,10H104,MECL AND GATES				3170073-00	1
U9		IC,3199E,VHF/UHF,4 PRESCALER				3043199-00	1
U10		IC,AD96685,ULTRAFAST COMPARATOR				3110126-00	1
U11		IC,SMD,74HC595,8-BIT SHIFT REGISTER				3170056-00	2
U12		IC,SMD,DG403DY				3110130-00	2
U13	U12						
U14		IC,AD1856,16-BIT PCM AUDIO DAC				3110129-00	1
U15		IC,SMD,OP-27,OP AMPL,S08				3170045-00	2
U16	U15						
U17		IC,SMD,NE521				3170028-00	4
U18	U17						

A9 SIGNAL CONDITIONER (Continued) 2020395-10 Rev. E

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
U19	U17			
U20	U17			
U21		IC,SMD,AD849JR,OP AMP,HI-SP,LO-PWR	3170082-00	1
U22		PAL,PRGM,16L8,DECODER	2070086-00	1
U23		IC,SMD,74LS279A,QUAD S-RFF	3170080-00	2
U24	U23			
U25		IC,SMD,74HC165,SHIFT REGISTER	3170078-00	1
U26	U11			
U27		IC,SMD,74S00,QUAD 2-INPUT NAND GATE	3170079-00	1
U28		IC,SMD,74HC125,QUAD 3-STATE	3110127-00	1
U29		IC,SMD,10H125,MECL/TTL TRANSLATOR	3170070-00	1
U30		NOT USED		
U31	U4			
XU9		CONN,SOCKET,DIP,8 PIN	2630014-00	1
HARDWARE USED IN THIS ASSEMBLY				
		HANDLE,PCB	5230001-00	2
		PIN,ROLL,3/32 DIA 1/4 LG	5110008-00	2
		PCB SCHEMATIC DIAGRAM	5500395-10 B	REF.

COMPONENT COORDINATES (SIGNAL CONDITIONER ASSEMBLY A9)

REF DES	COORD	REF DES	COORD	REF DES	COORD	REF DES	COORD	REF DES	COORD
C1	A-1	C62	A-10	L1	A-2	R50	A-3	R117	C-4
C2	A-2	C63	B-10	L2	B-1	R51	A-3	R118	C-4
C3	B-1	C64	B-11	L3	C-1	R52	B-4	R119	C-12
C4	B-1	C65	B-11	L4	D-1	R53	C-4	R121	D-2
C5	B-1	C66	B-4	L5	A-2	R54	C-4	R122	C-3
C6	B-2	C67	C-4	L6	B-2	R55	C-3	R123	B-7
C7	C-1	C68	C-5	L7	D-2	R56	C-4	R124	B-7
C8	C-2	C69	A-11	L8	D-2	R57	D-2	R125	B-8
C9	C-1	C70	A-12	L9	C-3	R58	C-4	R126	D-2
C10	C-2	C71	C-12	L10	B-7	R59	C-3	R127	A-3
C11	D-2	C72	C-12	L11	D-2	R60	C-4	R128	C-3
C12	D-1	C73	C-12			R61	C-4		
C13	D-2	C74	C-11	Q1	B-12	R62	C-4	TP1	C-2
C14	A-2	C75	C-2	Q2	B-12	R63	D-4	TP2	D-3
C15	A-2	C76	D-2			R64	D-4	TP3	D-5
C17	A-2	C77	B-11	R1	A-1	R65	D-4	TP4	A-1
C18	B-2	C78	B-12	R2	A-1	R66	B-5	TP5	B-2
C19	B-2	C79	C-11	R3	A-1	R67	C-5	TP6	A-4
C20	B-2	C80	A-7	R4	B-1	R68	C-6	TP7	C-5
C21	B-2	C81	B-7	R5	B-1	R69	C-5	TP8	B-7
C22	C-2	C82	B-7	R6	B-1	R70	C-5	TP9	C-9
C23	C-3	C83	B-7	R7	B-1	R71	A-7		
C25	D-2	C84	D-9	R8	B-1	R72	C-5	U1	A-2
C26	A-3	C85	D-9	R9	C-1	R73	A-7	U2	A-2
C27	B-2	C86	D-9	R10	C-1	R74	A-8	U3	B-2
C29	C-3	C87	D-5	R11	C-1	R75	A-8	U4	C-1
C30	C-3	C88	D-11	R12	D-1	R76	A-8	U5	C-2
C31	C-3	C90	B-3	R13	D-1	R77	B-8	U6	D-2
C32	C-2	C91	B-8	R14	D-1	R78	B-8	U7	B-3
C33	B-8	C92	C-2	R15	D-1	R79	B-8	U8	C-3
C34	D-3	C93	D-3	R16	D-1	R81	A-8	U9	C-3
C35	D-3			R17	B-2	R83	A-9	U10	D-3
C36	B-3	CR1	B-1	R18	B-2	R84	A-11	U11	A-4
C37	B-3	CR2	B-2	R19	A-1	R88	C-5	U12	B-4
C38	C-4	CR3	B-2	R20	B-2	R89	D-3	U13	C-4
C39	C-3	CR4	C-2	R21	B-2	R90	A-2	U14	B-5
C40	D-3	CR5	C-2	R22	B-2	R91	A-2	U15	B-5
C41	D-4	CR6	C-2	R23	B-2	R92	A-2	U16	C-5
C42	A-4	CR7	C-2	R24	B-2	R93	A-12	U17	A-7
C43	B-5	CR8	C-2	R25	B-1	R94	A-12	U18	A-8
C44	B-4	CR9	C-2	R26	B-2	R95	B-12	U19	B-8
C45	D-4	CR10	C-2	R27	C-2	R96	B-12	U20	B-8
C46	A-5	CR12	D-2	R28	C-2	R97	B-12	U21	B-7
C47	B-5	CR14	B-3	R29	C-2	R98	B-12	U22	C-8
C48	C-6	CR15	B-3	R30	C-2	R99	B-12	U23	A-9
C49	C-5	CR17	C-11	R31	C-1	R101	C-11	U24	B-9
C50	A-7	CR19	B-12	R32	D-2	R102	C-12	U25	C-9
C51	A-7	CR20	C-3	R35	D-2	R103	C-12	U26	A-10
C52	A-8	CR21	C-4	R37	C-2	R104	C-12	U27	B-10
C53	B-9	CR22	C-4	R38	D-2	R105	C-11	U28	C-10
C54	B-9			R40	B-3	R106	D-11	U29	A-11
C55	C-7	J1	A-2	R41	B-3	R110	B-7	U31	C-11
C56	A-9	J2	A-2	R42	B-3	R112	C-7		
C57	B-9	J3	A-3	R44	C-3	R113	B-7	W1	D-10
C58	B-9	J5	A-4	R45	C-3	R114	B-7	W2	D-10
C59	C-8	J6	A-7	R46	C-3	R115	A-11	W3	C-10
C60	C-9	J7	A-3	R48	D-3	R116	B-4	W4	C-10
C61	C-10	J8	A-11	R49	A-3				

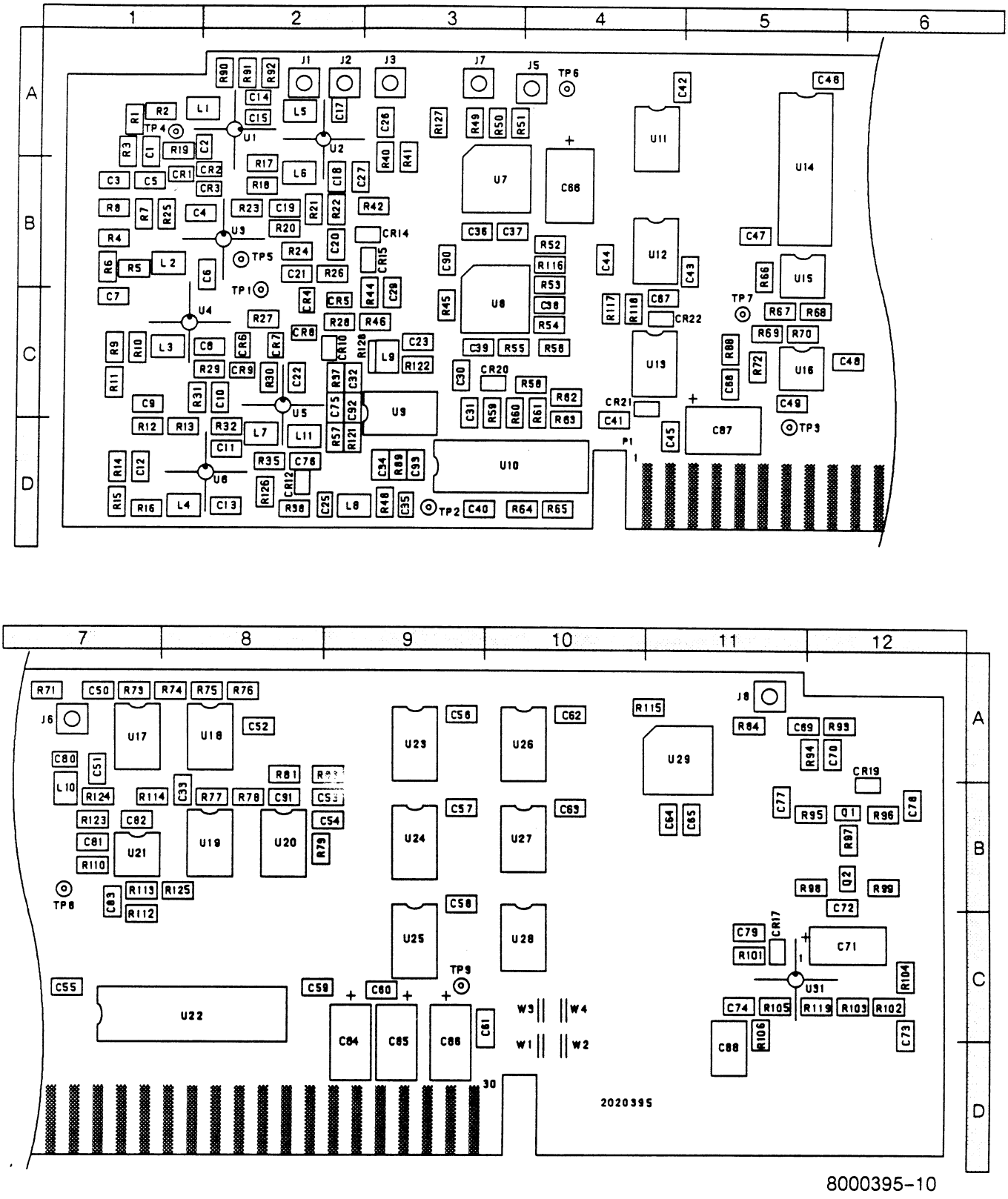


Figure 10-24. Signal Conditioner (A9) Component Locator.

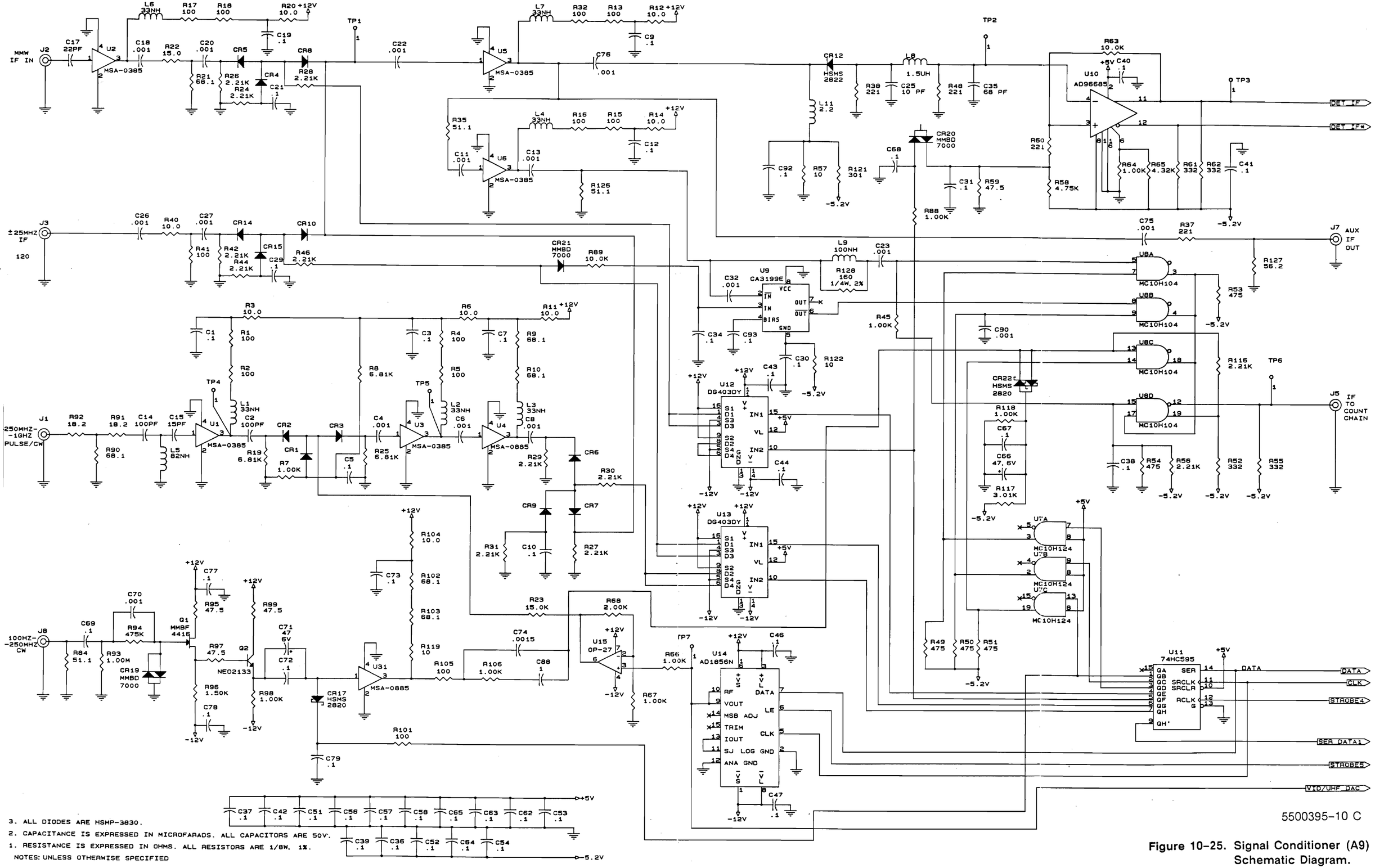


Figure 10-25. Signal Conditioner (A9) Schematic Diagram. (Sheet 1 of 2)

IC NO.	IC TYPE	IC PINS				
		GND	+5V	-5.2V	+12V	-12V
U27	74S00	8	14			
U23, U24	74LS279	8	16			
U11, U26	74HC595	8	16			
U25	74HC165	8	16			
U28	74HC125	7	14			
U22	16L8	10	20			
U8	MC10H104	2, 20		10		
U4, U31	MSA-0885	2, 4				
U7	MC10H124	20	12	10		
U29	MC10H125	20	12	10		
U21	AD849JR				7	4
U10	AD96685	1, 16	2	8		
U17, U18, U19, U20	NE521	7	6, 14	13		
U15, U16	OP-27				7	4
U12, U13	DG403DY	13	12		11	14
U14	AD1856	2, 12			3, 16	1, 8
U9	CA3199E	8		5		
U1, U2, U3, U5, U6	MSA-0385	2, 4				

LAST USED	NOT USED
C93	C16
R128	R39, R80, R82, R85, R86, R87, R100, R107, R108, R109
CR22	CR18
L11	
U31	U30
J8	
P1	
TP9	
Q2	

5500395-10 C

Figure 10-25. Signal Conditioner (A9) Schematic Diagram. (Sheet 2 of 2)

A10
BAND 2 MICROWAVE CONVERTER
(2010936-02 Rev. A) 585B
(2010936-01 Rev. B) 588B

NOTE

Due to the extensive test equipment and special processes required to test and repair this assembly, field repair of this assembly is not recommended. For this reason the information contained in this section is limited to what is necessary for troubleshooting to the assembly level. Exchange modules are available from EIP. Please consult the factory for pricing.

CAUTION

Attempted disassembly or repair of the microwave converter will void warranty and prevent the unit from being accepted for module exchange or repair.

The Band 2 microwave converter is a complete microwave downconverter consisting of five subassemblies: YIG, VCO, AFC, IF, and YTF driver.

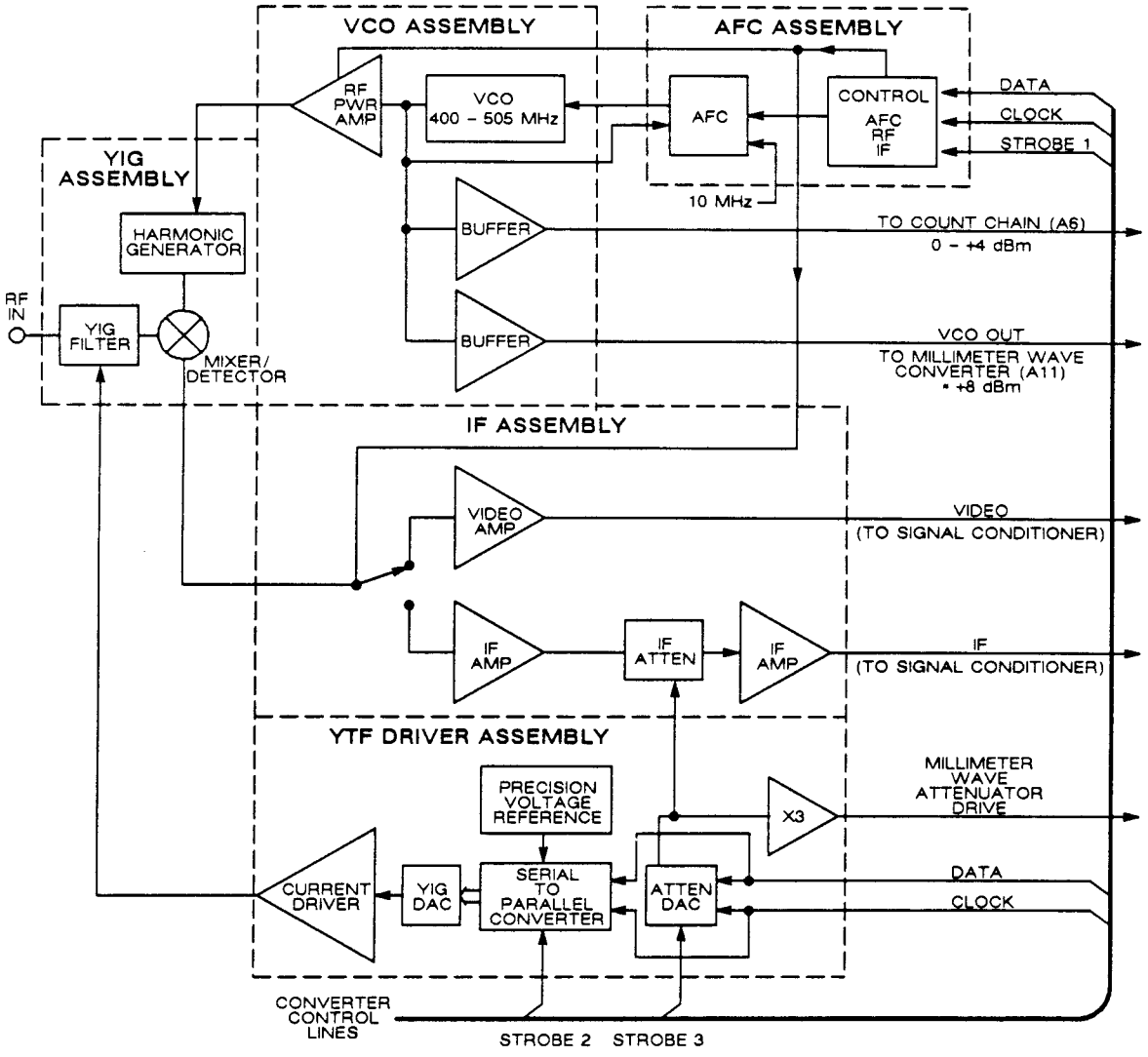


Figure 10-26. Band 2 Converter Block Diagram.

The YIG assembly consists of the YIG filter, harmonic generator, and mixer. The YIG filter is an electronically tunable, narrow bandpass microwave filter having a bandpass of approximately 25 MHz and a rolloff of approximately 12 dB per octave. The filter eliminates all but the desired signal from reaching the input mixer. The harmonic generator receives its input from the synthesized VCO signal and generates harmonics of the VCO signal. One of these harmonics mixes with the incoming signal to produce the IF signal.

The VCO assembly contains a 400 to 505 MHz voltage controlled oscillator, a power amplifier, and two buffer amplifiers. The power amplifier boosts the VCO output power to approximately +28 dBm and is used to drive the harmonic generator.

The AFC assembly consists of AFC and VCO frequency control circuitry. The AFC assembly along with the VCO form a programmable phase lock loop that allows the VCO frequency to be precisely set, in 100 kHz increments, from 400 to 505 MHz.

The IF/video amplifier assembly contains the video amplifier, two IF amplifiers, and a variable IF attenuator. This assembly allows the IF signal level to be adjusted to the optimum level for counting and amplifying the video signal.

The YTF driver allows microprocessor control of the YIG filter, IF attenuator, and millimeter wave IF attenuator. Technical information on the YTF driver is presented in this section to allow troubleshooting of problems between the main counter and the Band 2 microwave converter.

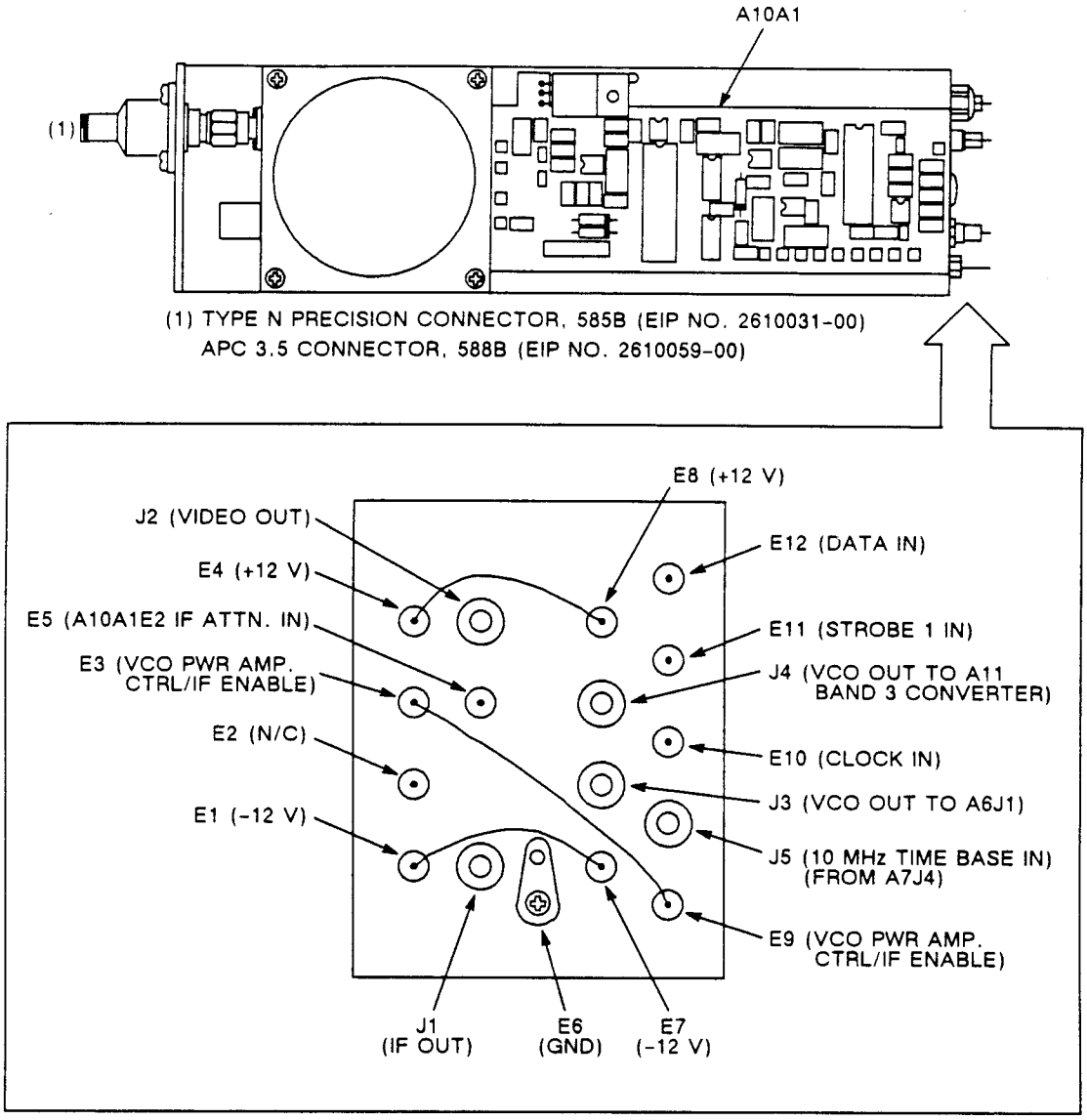
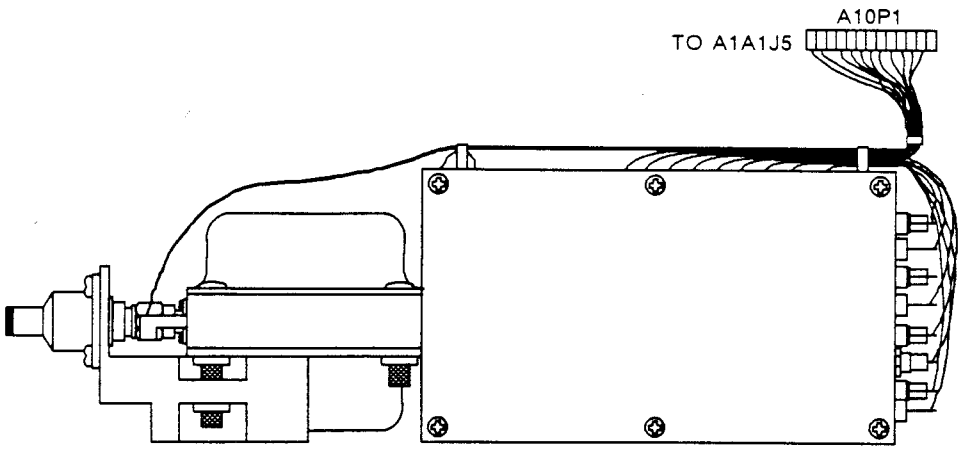


Figure 10-27. Band 2 Converter (588B Shown).



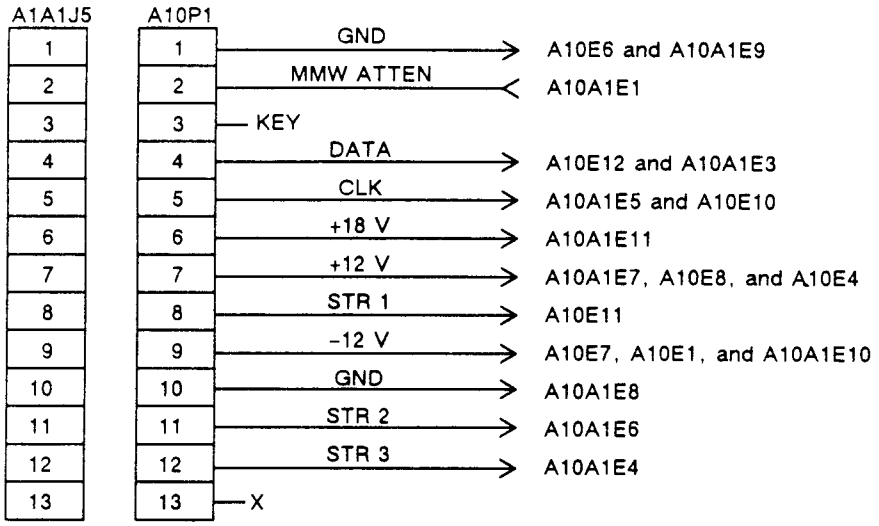


Figure 10-28. Band 2 Converter Interconnections (588B Shown).

A10A1
YTF DRIVER
(2020452-03)

The YTF driver serves three major functions:

1. Converts serial data from the microprocessor into the current drive required to tune the YIG filter.

2. Converts serial data from the microprocessor into the voltage required to adjust the Band 2 IF attenuator.

3. Converts serial data from the microprocessor into the voltage required to adjust the Band 3 IF attenuator.

The first two functions are used only during Band 2 operation, and the third is used only during Band 3 operation.

When tuning the YIG filter, serial data from the D0 line of the microprocessor data bus is applied to a serial to parallel shift register U5 and U6 at pin 14. An active high latch enable on U5 and U6 at pin 12 causes the data to be latched at the outputs and applied to the inputs of U7, a 16-bit DAC. A precision 7 volt reference voltage for the DAC is supplied by U3, U4, and the associated components.The DAC converts the data into an output current which is applied to U8, a current-to-voltage converter. The output voltage from U8 is applied to U9, the first stage of the current driver. The normally positive output voltage from U9 is prevented from going negative, more than 0.7 volts, by the combination of R17 and CR4. The output voltage from U9 is applied to Q2, a unity gain buffer/driver. The output from the collector of Q2 supplies base current to Q3, a current driver, which in turn supplies current to the YIG tuning coil. The resulting YIG current is sensed by resistor R15 and applied as feedback to U9, limiting the current at the required value. When the current to the YIG filter is turned off, the resulting flyback voltage is limited to approximately 51.7 volts by the combination of CR2 and zener diode CR3.

To adjust either the Band 2 IF attenuator or the Band 3 IF attenuator, serial data from the D0 line of the microprocessor data bus is applied to the attenuator DAC U2 at pin 7. An active high latch enable signal on U2 pin 6 causes the data to be read into the DAC. The DAC converts the data into an analog output voltage. For Band 2 operation, this voltage controls the Band 2 IF attenuator. For Band 3 operation, this voltage is amplified by a factor of three, by U1, and applied to the Band 3 IF attenuator.

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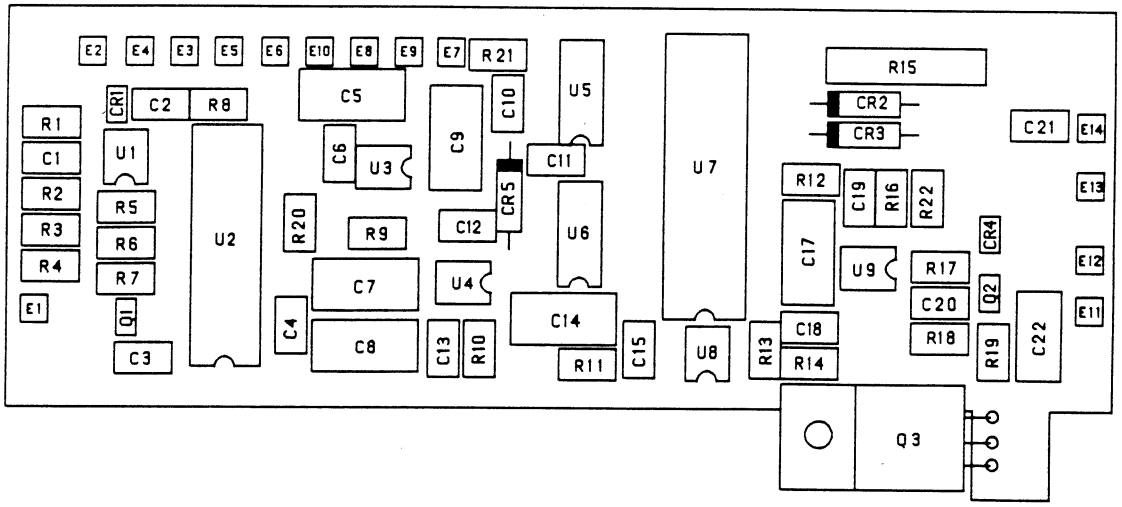
A10A1 YTF DRIVER 2020452-03 Rev. D

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,SMD,Z5U	.1µF	20%	50V	2100046-00	13
C2	C1						
C3	C1						
C4	C1						
C5		CAP,SMD,TANT	10µF	10%	25V	2100043-00	6
C6	C1						
C7	C5						
C8	C5						
C9	C5						
C10	C1						
C11	C1						
C12	C1						
C13	C1						
C14	C5						
C15	C1						
C16		NOT USED					
C17	C5						
C18	C1						
C19	C1						
C20	C1						
C21		CAP,SMD,CER,NPO	470PF	5%	50V	2100033-00	1
C22		CAP,SMD,Z5U	1µF	20%	50V	2100108-00	1
CR1		DIODE,SMD,MMBD7000				2740010-00	2
CR2		DIODE,1N4003,GP RECTIFIER				2700004-00	1
CR3		DIODE,1N5369A ZENER,51V,5.0W				2700008-00	1
CR4	CR1						
CR5		DIODE,1N5232B,ZENER 5.6V,5%				2735232-00	1
Q1		XSTR,SMD,MMBT4124,SOT-23				4730012-00	2
Q2	Q1						
Q3		XSTR,PWR,TIP127,TO-220				4710057-00	1
R1		RES,SMD	392	1/8W	1%	4233920-00	4
R2	R1						
R3	R1						
R4	R1						
R5		RES,SMD	2.00K	1/8W	1%	4232001-00	1
R6		RES,SMD	1K	1/8W	1%	4231001-00	5
R7		RES,SMD	100	1/8W	1%	4231000-00	4
R8	R6						
R9		RES,SMD	10K	1/8W	1%	4231002-00	3
R10	R7						
R11	R7						
R12	R9						
R13		RES,SMD	40.2K	1/8W	1%	4234022-00	1
R14	R7						
R15		RES,PRECISION	5.0	3W	1%	4120023-00	1
R16	R9						
R17	R6						
R18	R6						
R19	R6						
R20		JUMPER,SMD MINI MCR18				5000288-00	1
R21		RES,SMD	2.21K	1/8W	1%	4232211-00	1
R22		RES,SMD	5.11K	1/8W	1%	4235111-00	1
U1		IC,SMD,OP-27,OP AMPL,S08				3170045-00	2
U2		IC,AD1856,16-BIT PCM AUDIO DAC				3110129-00	1
U3		IC,SMD,LT1021-7,7V,PRECISION REF				3170132-00	1
U4		IC,SMDOP-177,PRECISION OP AMP				3170131-00	2
U5		IC,SMD,74HC595,8-BIT SHIFT REGISTER				3170056-00	2
U6	U5						
U7		IC,HS3160,MONOLITHIC,16-BIT,MDAC				3077439-00	1
U8	U4						
U9	U1						
		PCB SCHEMATIC DIAGRAM				5500452-03 D	REF.



8000452-03

Figure 10-29. YTF Driver (A10A1) Component Locator.

IC POWER CHART				
IC NO.	IC PINS			
	GND	+5.6V	+12V	-12V
U1			(7)	4
U2	2, 12		(3, 16)	1, 8
U3	4		2	
U4	4		(7)	
U5	8	16		
U6	8	16		
U7	3		(20)	
U8			(7)	(4)
U9			7	4

LAST USED	NOT USED
C22	C16
R22	
U9	
CR5	
Q3	
E14	

THIS GROUND POINT IS ALSO CONNECTED TO THE CONVERTER HOUSING THROUGH A BOARD MOUNTING SCREW. ALL OTHER MOUNTING SCREWS ARE GROUND ISOLATED.

2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W, 1%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500452-03 D

Figure 10-30. YTF Driver (A10A1) Schematic Diagram.

A10
BAND 2 MICROWAVE CONVERTER
(2010670-01 Rev. A) 585B
(2010670-02 Rev. A) 588B

NOTE

Due to the extensive test equipment and special processes required to test and repair this assembly, field repair of this assembly is not recommended. For this reason the information contained in this section is limited to what is necessary for troubleshooting to the assembly level. Exchange modules are available from EIP. Please consult the factory for pricing.

CAUTION

Attempted disassembly or repair of the microwave converter will void warranty and prevent the unit from being accepted for module exchange or repair.

The Band 2 microwave converter is a complete microwave downconverter consisting of five subassemblies: YIG, VCO, AFC, IF, and YTF driver.

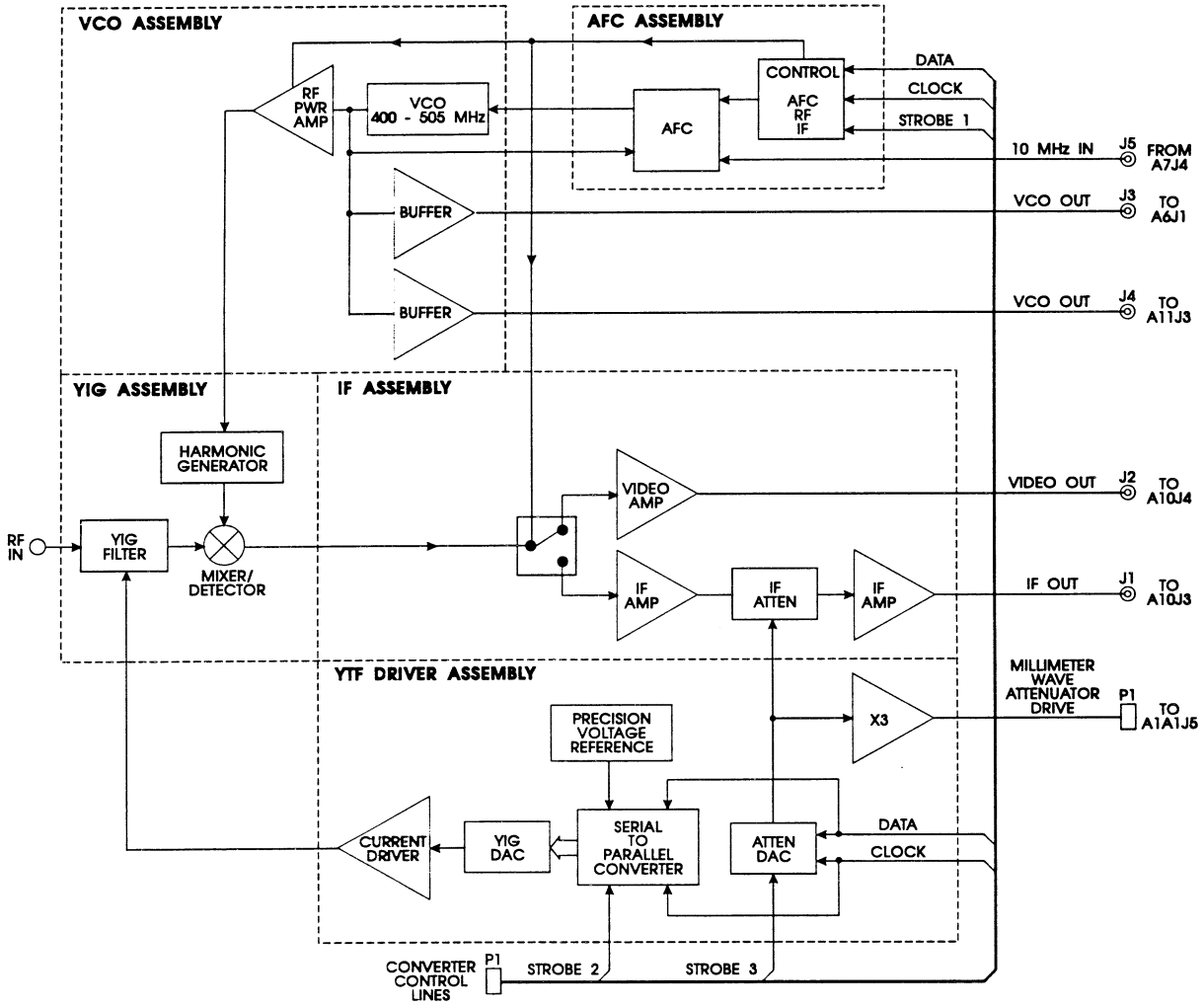


Figure 10-30A. Band 2 Converter Block Diagram.

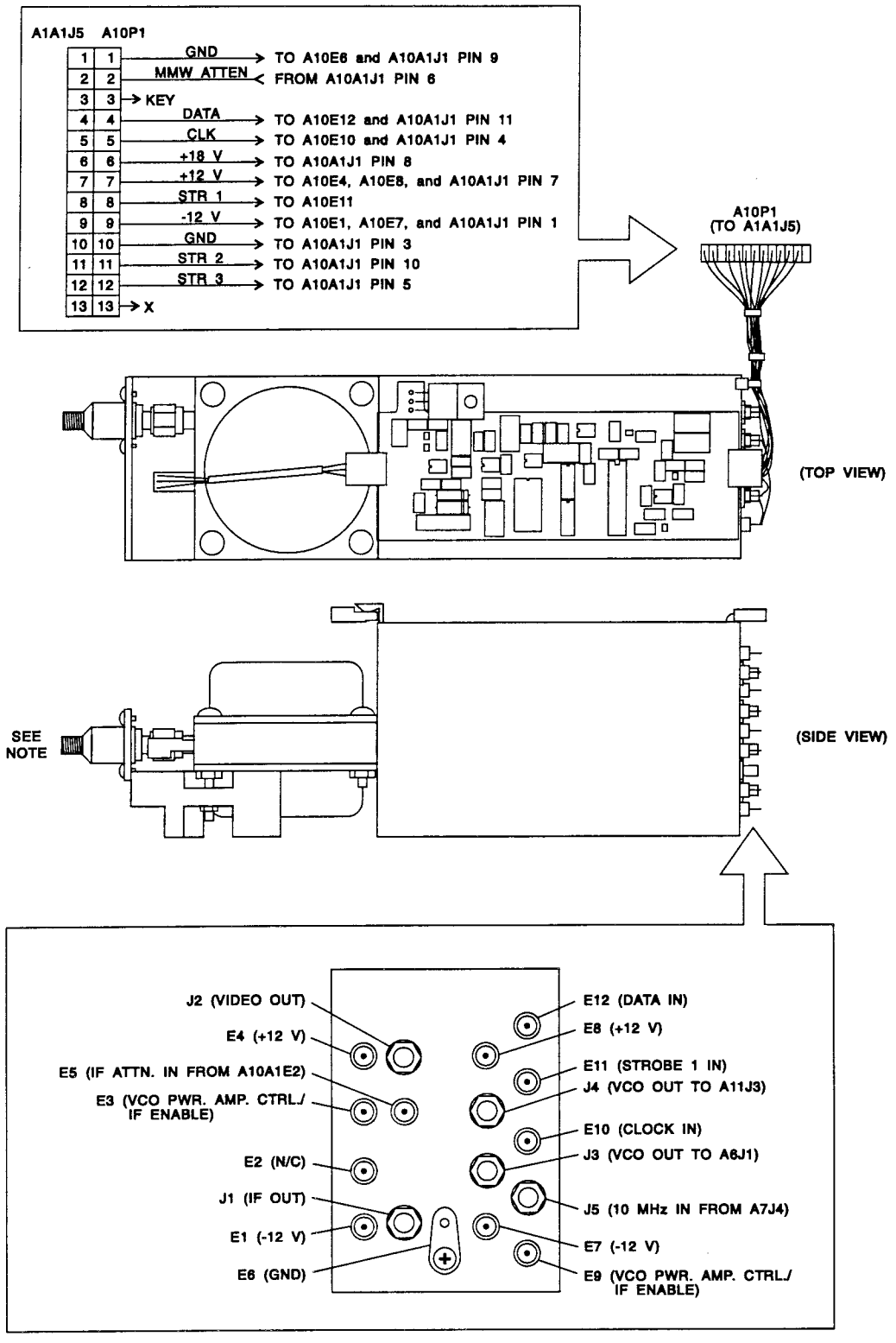
The YIG assembly consists of the YIG filter, harmonic generator, and mixer. The YIG filter is an electronically tunable, narrow bandpass microwave filter having a bandpass of approximately 25 MHz and a rolloff of approximately 12 dB per octave. The filter eliminates all but the desired signal from reaching the input mixer. The harmonic generator receives its input from the synthesized VCO signal and generates harmonics of the VCO signal. One of these harmonics mixes with the incoming signal to produce the IF signal.

The VCO assembly contains a 400 to 505 MHz voltage controlled oscillator, a power amplifier, and two buffer amplifiers. The power amplifier boosts the VCO output power to approximately +28 dBm and is used to drive the harmonic generator.

The AFC assembly consists of AFC and VCO frequency control circuitry. The AFC assembly along with the VCO form a programmable phase lock loop that allows the VCO frequency to be precisely set, in 100 kHz increments, from 400 to 505 MHz.

The IF/video amplifier assembly contains the video amplifier, two IF amplifiers, and a variable IF attenuator. This assembly allows the IF signal level to be adjusted to the optimum level for counting and amplifying the video signal.

The YTF driver allows microprocessor control of the YIG filter, IF attenuator, and millimeter wave IF attenuator. Technical information on the YTF driver is presented in this section to allow troubleshooting of problems between the main counter and the Band 2 microwave converter.



NOTE: TYPE N PRECISION CONNECTOR, 585B (EIP NO. 2610031-00)
APC 3.5 CONNECTOR, 588B (EIP NO. 2610059-00)

Figure 30B. Band 2 Converter (588B Shown).

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A10A1
YTF DRIVER
(2020483-02)

The YTF driver serves three major functions:

1. Converts serial data from the microprocessor into the current drive required to tune the YIG filter.
2. Converts serial data from the microprocessor into the voltage required to adjust the Band 2 IF attenuator.
3. Converts serial data from the microprocessor into the voltage required to adjust the Band 3 IF attenuator

The first two functions are used only during Band 2 operation, and the third is used only during Band 3 operation.

When tuning the YIG filter, serial data from the D0 line of the microprocessor data bus is applied to a serial to parallel shift register U4 and U5 at pin 14. An active high latch enable on U5 and U6 at pin 12 causes the data to be latched at the outputs and applied to the inputs of U7, a 16-bit DAC. A precision 7 volt reference voltage for the DAC is supplied by U3, U6, and the associated components. The DAC converts the data into an output current which is applied to U8, a current-to-voltage converter. The output voltage from U8 is applied to U9, the first stage of the current driver. The normally positive output voltage from U9 is prevented from going negative, more than 0.7 volts, by the combination or R18 and CR5. The output voltage from U9 is applied to Q2, a unity gain buffer/driver. The output from the collector of Q2 supplies base current to Q3, a current driver, which in turn supplies current to the YIG tuning coil. The resulting YIG current is sensed by resistor R14 and applied as feedback to U9, limiting the current at the required value. When the current to the YIG filter is turned off, the resulting flyback voltage is limited to approximately 51.7 volts by the combination of CR4 and zener diode CR3.

To adjust either the Band 2 IF attenuator or the Band 3 IF attenuator, serial data form the D0 line of the microprocessor data bus is applied to the attenuator U2 at pin 7. An active high latch enable signal on U2 pin 6 causes the data to be read into the DAC. The DAC converts the data into an analog output voltage. For Band 2 operation, this voltage controls the Band 2 IF attenuator. For Band 3 operation, this voltage is amplified by a factor of three, by U1, and applied to Band 3 IF attenuator.

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A10A1 YTF DRIVER — 2020483-02 Rev. A

ITEM NO.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,SMD,TANT	10µF	20%	25V	2130106-25	6
C2	C1						
C3		CAP,SMD,Z5U,1206,	.10µF	20%		2270104-00	13
C4	C3						
C5	C3						
C6	C3						
C7	C3						
C8	C3						
C9	C3						
C10	C1						
C11	C3						
C12	C3						
C13	C1						
C14	C1						
C15	C3						
C16	C3						
C17	C1						
C18	C3						
C19	C3						
C20		CAP,SMD,NPO,1206	470PF	5%		2190471-00	1
C21		CAP,SMD,Z5U	1µF	20%	50V	2100108-00	1
CR1		DIODE,SMD,MMBD7000				2740010-00	2
CR2		DIODE,SMD,MMBZ5232B,ZENER,5.6V				2740024-00	1
CR3		DIODE,1N5369A,ZENER,51V,5.0W				2700008-00	1
CR4		DIODE,1N4003,GP RECTIFIER				2700004-00	1
CR5	CR1						
J1		CONN,HEADER,2X6 PIN,.10CTR,RT.ANGL				2620357-00	1
J2		CONN,HEADER,5 PIN RT ANG,100 CTRS				2620348-00	1
Q1		XSTR,SMD,MMBT4124,SOT-23				4730012-00	2
Q2	Q1						
Q3		XSTR,PWR,TIP127,TO-220				4710057-00	1
R1		RES,SMD	392	1/8W	1%	4233920-00	4
R2	R1						
R3		RES,SMD	100	1/8W	1%	4231000-00	4
R4	R1						
R5		RES,SMD	1K	1/8W	1%	4231001-00	5
R6	R1						
R7	R5						
R8		RES,SMD	2.00K	1/8W	1%	4232001-00	1
R9		RES,SMD	2.21K	1/8W	1%	4232211-00	1
R10		RES,SMD	10K	1/8W	1%	4231002-00	3
R11	R3						
R12	R3						
R13		RES,SMD	40.2K	1/8W	1%	4234022-00	1
R14		RES,PWR,PRECISION	5.0	3W	1%	4120023-00	1
R15	R3						
R16	R10						
R17		RES,SMD	5.11K	1/8W	1%	4235111-00	1
R18	R5						
R19	R10						
R20	R5						
R21	R5						
U1		IC,SMD,OP-27,OP AMPL,S08				3170045-00	2
U2		IC,AD1856,16-BIT PCM AUDIO DAC				3110129-00	1
U3		IC,SMD,LT1021-7,7V,PRECISION REF			3170132-00	1	
U4		IC,SMD,74HC595,8-BIT SHIFT REGISTER				3170056-00	2
U5	U4						
U6		IC,SMDOP-177,PRECISION OP AMP				3170131-00	2
U7		IC,SMD,SP7516,ML 16-BIT MDAC				3170154-00	1
U8	U6						
U9	U1						
		PCB SCHEMATIC DIAGRAM				5500483-02	REF.

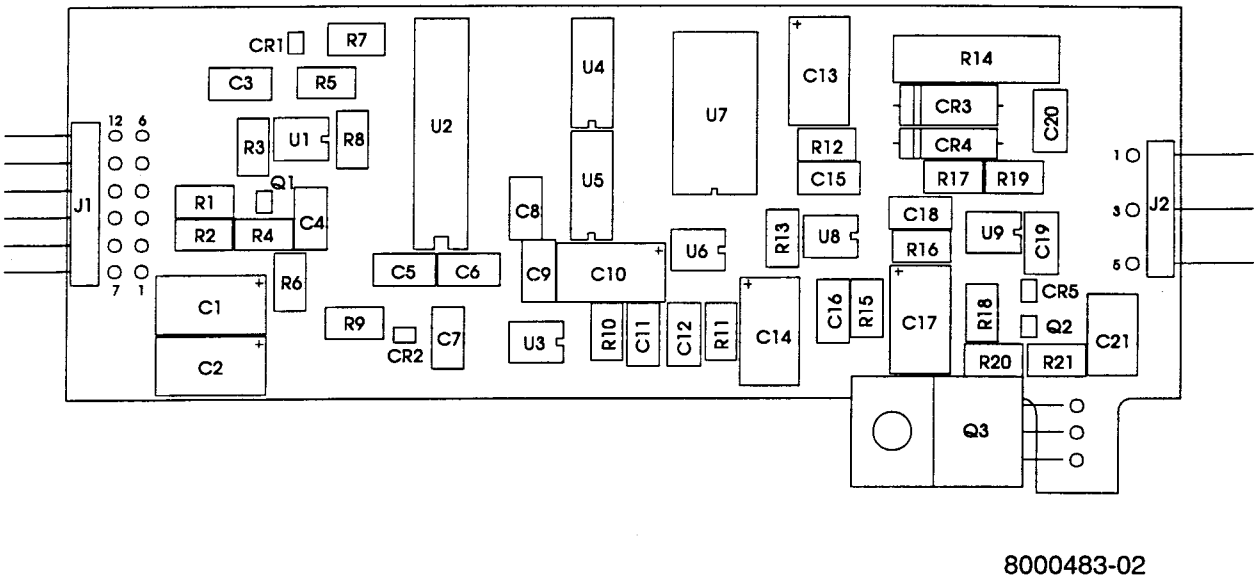
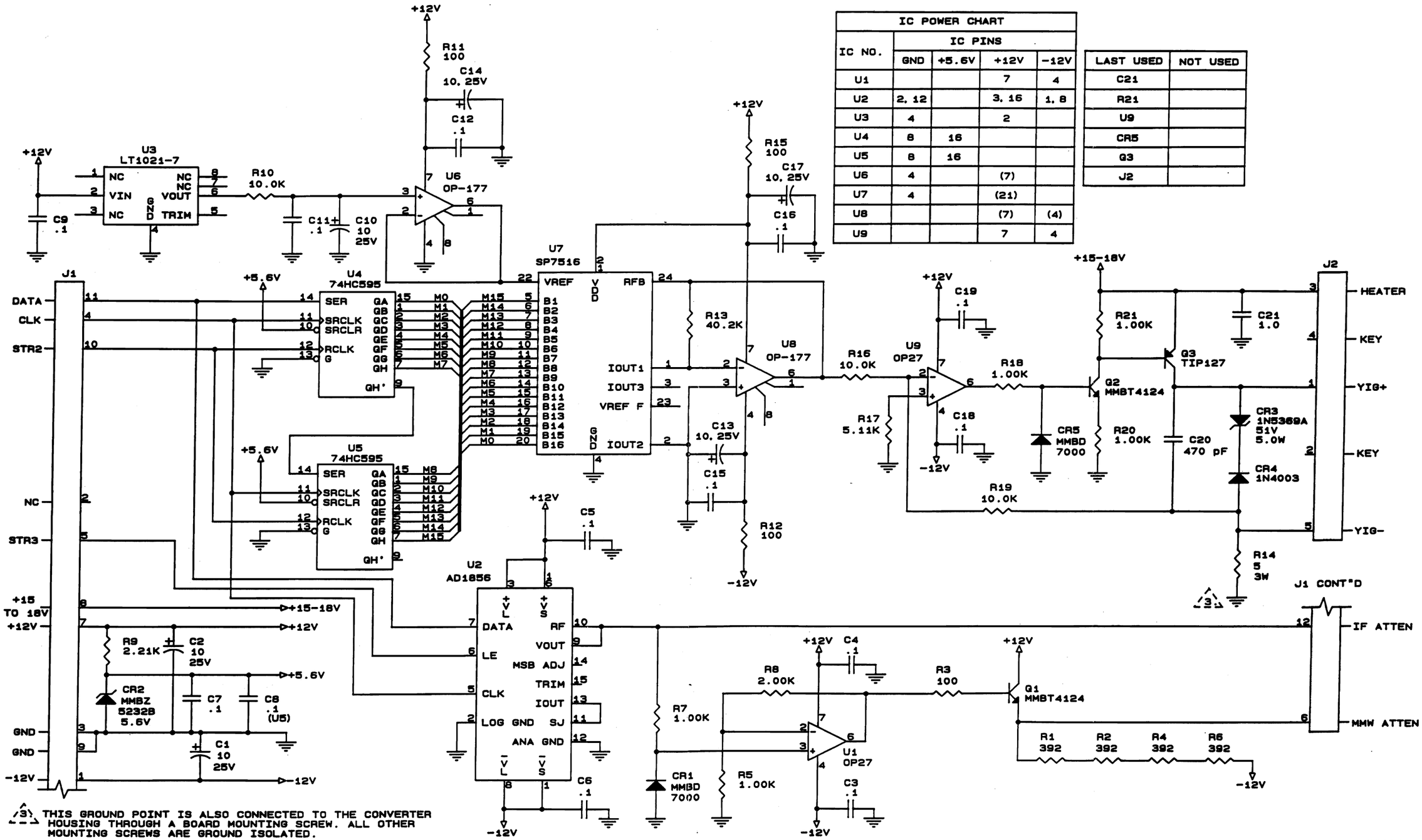


Figure 10-30C. YTF Driver (A10A1) Component Locator.

IC POWER CHART				
IC NO.	IC PINS			
	GND	+5.6V	+12V	-12V
U1			7	4
U2	2, 12		3, 16	1, 8
U3	4		2	
U4	8	16		
U5	8	16		
U6	4		(7)	
U7	4		(21)	
U8			(7)	(4)
U9			7	4

LAST USED	NOT USED
C21	
R21	
U9	
CR5	
Q3	
J2	



⚠3 THIS GROUND POINT IS ALSO CONNECTED TO THE CONVERTER HOUSING THROUGH A BOARD MOUNTING SCREW. ALL OTHER MOUNTING SCREWS ARE GROUND ISOLATED.

2. CAPACITANCE IS EXPRESSED IN MICROFARADS. ALL CAPACITORS ARE 50V.

1. RESISTANCE IS EXPRESSED IN OHMS. ALL RESISTORS ARE 1/8W, 1%.

NOTES: UNLESS OTHERWISE SPECIFIED

5500483-02 A

Figure 10-30D. YTF Driver (A10A1) Schematic Diagram.

A12
FRONT PANEL
2010761-01

The front panel assembly consists of the front panel, the front panel controls, signal input connectors and two printed circuit boards (A12A1 and A12A2).

The display/keyboard assembly (A2A1) consists of a 12-digit numeric display along with the status indicators, segment drivers and keyboard.

The front panel logic assembly (A12A2) provides the electronic interface between the microprocessor and the display. All information between the microprocessor and the display assembly enters this board at P2.

To prevent digital noise created in the display from interfering with counter performance, a separate 5 V regulator is used for the front panel display. This regulator is mounted on the frame near the left side of the front panel and is to connected to the front panel at A12A2J5.

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A12 FRONT PANEL 2010761-01 Rev. G

ITEM NO.	DESCRIPTION	EIP NO.	UNITS PER ASSY
1	SAMPLE RATE ASSY	2010134-01	1
2	SWITCH ASSY	2040440-01	1
4	PCB ASSY,FR PNL DISPLAY/CONTROL	2020140-02	1
5	PCB ASSY,FR PNL LOGIC **(585B: CCN 6804 THRU 6806)** **(588B: CCN 6905 THRU 6908)**	2020191-01	1
	OR		
5	PCB ASSY,FR PNL LOGIC **(585B: CCN 6806)** **(588B: CCN 6908)**	2020191-02	1
10	NUT,KNURLED 3/8-32	5110026-00	1
12	PIN,ALIGNMENT,DISPLAY	5210190-00	2
13	RETAINER,KEY	5210191-00	1
14	BUTTON,SET (MF 5230005-02)	5210220-00	1
15	KNOB,MOD	5210223-00	1
20	TAPE,MASKING,ADHESIVE 2 SIDES	5601003-00	4 IN.
21	PANEL,FRONT	5210817-01	1
22	SCR,FLN,X-REC,100 DEG,4-40X5/16,UNC	5140004-05	2
23	SCR,PNH X-REC 4-40X1/2 UNC	5120004-08	9
24	WASHER,FLAT,CRES,REDUCED 0.D NO.4	5161004-00	10
25	WASH,LK,INTL-T,CRES #4	5163004-00	1
26	NUT,HEX,CRES 4-40 UNC-2B	5180004-40	1
27	DRESSNUT,CAPTIVATING	5000357-00	1
28	CABLE ASSY,COAX,A12W6	2040451-01	1
29	SRC ASSY,INPUT,B1	2040293-01	1

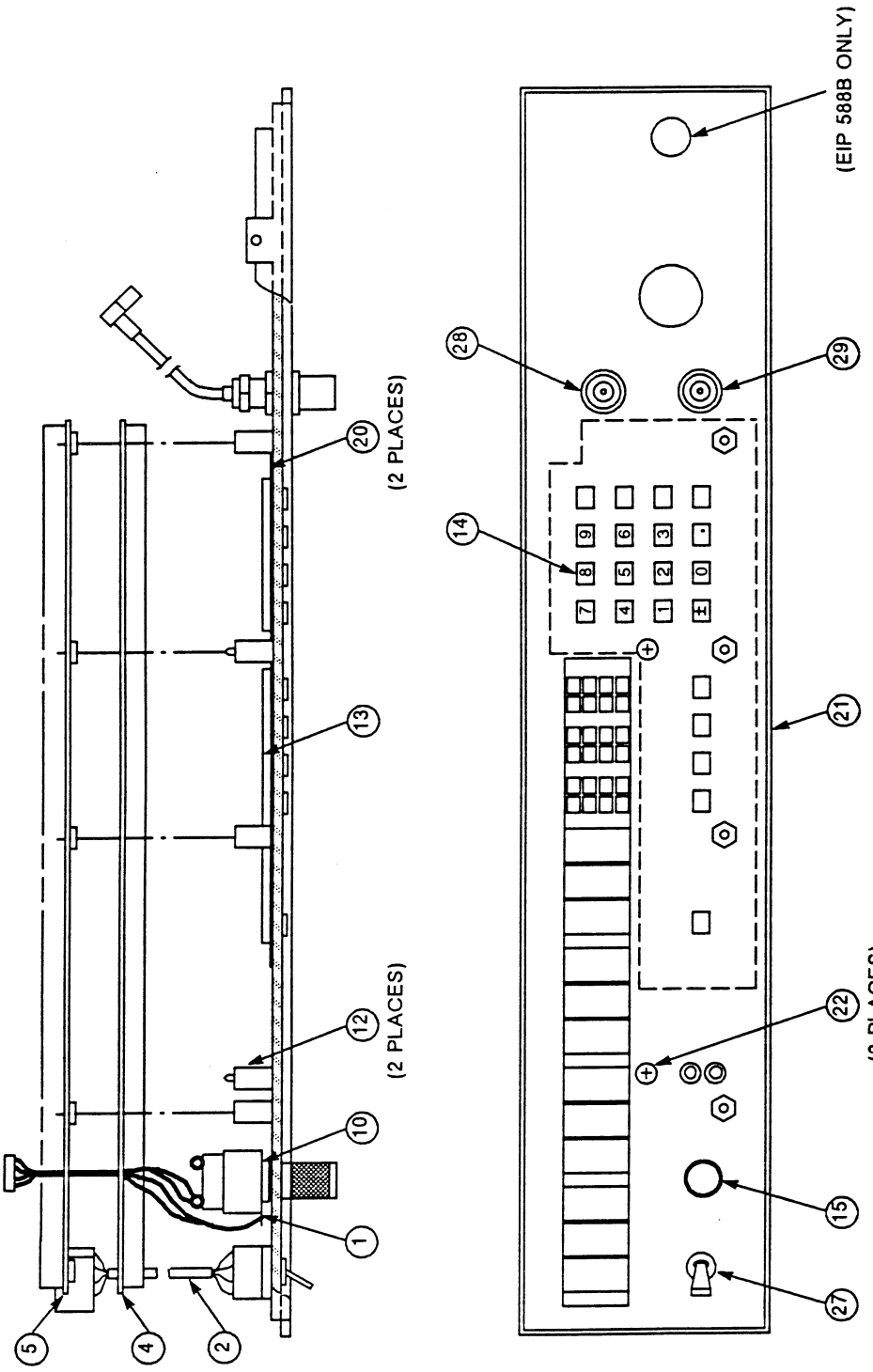


Figure 10-31. Front Panel (A12).

A12A1
FRONT PANEL DISPLAY and KEYBOARD
(2020140-02)

The front panel display and keyboard assembly is divided into two functional sections:

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains 12 common-anode, 7-segment numeric display units (DS1-DS12), 2 green LEDs (DS37 and DS38), and 24 yellow LEDs (DS13-DS36).

The 7-segment LEDs are mounted side by side, with space between each third digit from the right. The corresponding cathode segments are connected. The drive signals come from segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on front panel logic board (A12A2).

The two green LEDs (DS37 and DS38) are driven by Q1 and Q2. When these LEDs light, they indicate that the GATE or CONVERTER SEARCH modes are in operation.

The yellow LEDs (DS13-DS36) are divided into three groups of eight each. The anodes of all LEDs in each group are connected. The cathode of each grouped LED is connected to one of the segment drivers (Q3 through Q10). With this arrangement, each group of annunciator lights can be regarded as similar to one seven-segment LED. The digit drives for the three groups of annunciator lights also come from the front panel logic board.

KEYBOARD

This section of the assembly contains 21 single-pole, double-throw switches. The switches are arranged in a 4-row by 6-column matrix, with the extra switch taking the row 4, column 7 position. The columns are connected to +5 V through resistor network RN1 on the front panel logic board.

The keyboard is continuously scanned with signals derived from the front panel logic board. When the keyboard is being scanned, the four rows are grounded sequentially. When a row is grounded, and a key in that row is pressed, one of the columns will be grounded. This information is sent to the front panel logic board, where key debouncing is performed.

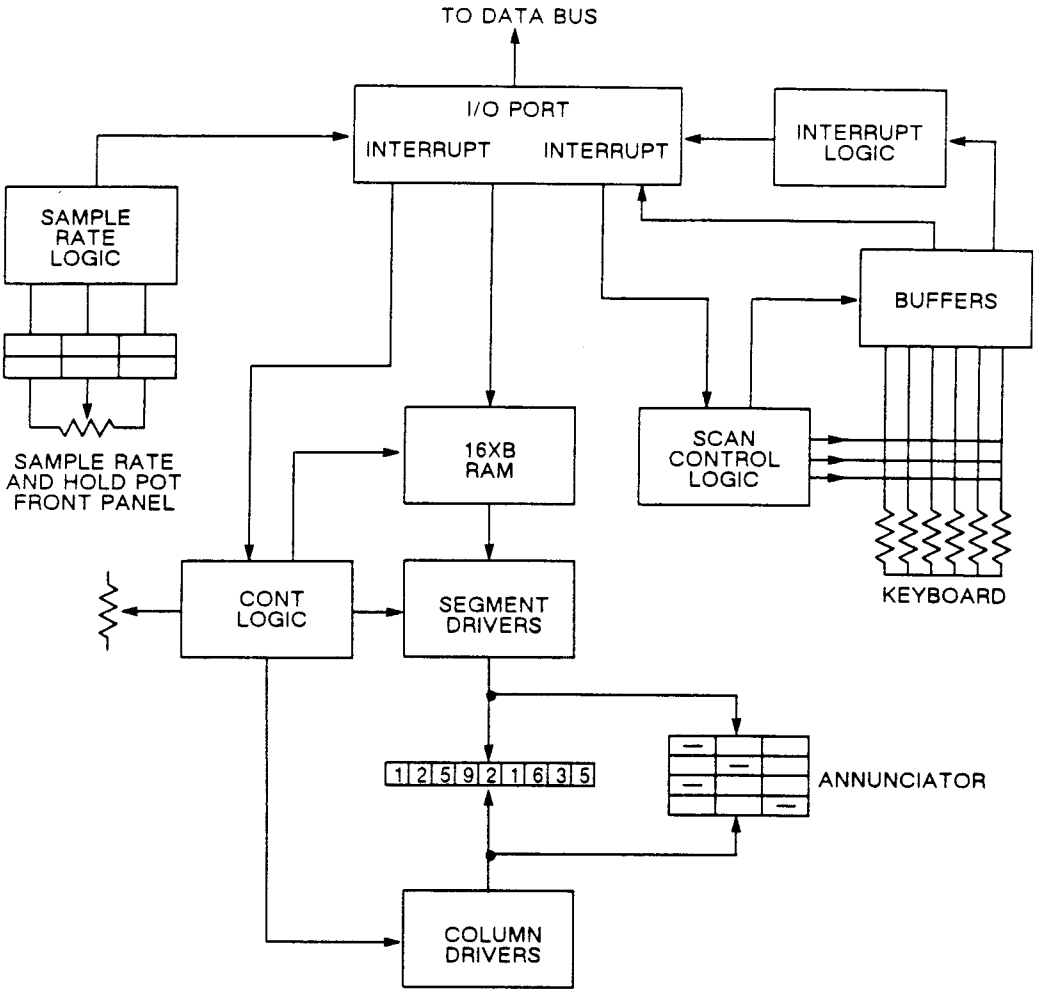


Figure 10-32. Front Panel Display and Logic Block Diagram.

A12A1 FRONT PANEL DISPLAY/KEYBOARD 2020140-02 Rev. D

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
DS1		LAMP,LED,NUMERIC INDICATOR				2800024-01	12
DS2	DS1						
DS3	DS1						
DS4	DS1						
DS5	DS1						
DS6	DS1						
DS7	DS1						
DS8	DS1						
DS9	DS1						
DS10	DS1						
DS11	DS1						
DS12	DS1						
DS13		LAMP,LED,YELLOW,RECT .15X.25				2800020-00	24
DS14	DS13						
DS15	DS13						
DS16	DS13						
DS17	DS13						
DS18	DS13						
DS19	DS13						
DS20	DS13						
DS21	DS13						
DS22	DS13						
DS23	DS13						
DS24	DS13						
DS25	DS13						
DS26	DS13						
DS27	DS13						
DS28	DS13						
DS29	DS13						
DS30	DS13						
DS31	DS13						
DS32	DS13						
DS33	DS13						
DS34	DS13						
DS35	DS13						
DS36	DS13						
DS37		LAMP,LED,GREEN,.12 OD				2800018-00	2
DS38	DS37						
P1		CONN,PCB RCPT,9 PIN				2620065-00	1
P2		CONN,PCB RCPT,17 PIN				2620067-00	1
P3		CONN,PCB RCPT,13 PIN				2620066-00	1
Q1		XSTR,2N4402,PNP,RF AMPLIFIER				4710019-00	10
Q2	Q1						
Q3	Q1						
Q4	Q1						
Q5	Q1						
Q6	Q1						
Q7	Q1						
Q8	Q1						
Q9	Q1						
Q10	Q1						
R1		RES,CC	4.7K	1/4W	5%	4010472-00	2
R2		RES,CC	130	1/4W	5%	4010131-00	2
R3	R1						
R4	R2						
R5		RES,CC	240	1/4W	5%	4010241-00	8
R6		RES,CC	18	1/4W	5%	4010180-00	8
R7	R5						
R8	R6						

A12A1 FRONT PANEL DISPLAY/KEYBOARD (Continued) 2020140-02 Rev. D

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
R9	R5			
R10	R6			
R11	R5			
R12	R6			
R13	R5			
R14	R6			
R15	R5			
R16	R6			
R17	R5			
R18	R6			
R19	R5			
R20	R6			
S1		SWITCH,MOM SPDT	4500013-00	21
S2		NOT USED		
S3		NOT USED		
S4		NOT USED		
S5		NOT USED		
S6	S1			
S7	S1			
S8	S1			
S9	S1			
S10	S1			
S11	S1			
S12	S1			
S13	S1			
S14	S1			
S15	S1			
S16	S1			
S17	S1			
S18	S1			
S19	S1			
S20	S1			
S21	S1			
S22	S1			
S23	S1			
S24	S1			
S25	S1			
XDS1		CONN,SOCKET,DIP,14 PIN	2630015-00	12
XDS2	XDS1			
XDS3	XDS1			
XDS4	XDS1			
XDS5	XDS1			
XDS6	XDS1			
XDS7	XDS1			
XDS8	XDS1			
XDS9	XDS1			
XDS10	XDS1			
XDS11	XDS1			
XDS12	XDS1			
XDS13		CONN,IC PIN(MINISERT)	2620054-00	48
XDS14	XDS13			
XDS15	XDS13			
XDS16	XDS13			
XDS17	XDS13			
XDS18	XDS13			
XDS19	XDS13			
XDS20	XDS13			
XDS21	XDS13			
XDS22	XDS13			

A12A1 FRONT PANEL DISPLAY/KEYBOARD (Continued) 2020140-02 Rev. D

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
XDS23	XDS13			
XDS24	XDS13			
XDS25	XDS13			
XDS26	XDS13			
XDS27	XDS13			
XDS28	XDS13			
XDS29	XDS13			
XDS30	XDS13			
XDS31	XDS13			
XDS32	XDS13			
XDS33	XDS13			
XDS34	XDS13			
XDS35	XDS13			
XDS36	XDS13			
HARDWARE USED IN THIS ASSEMBLY				
		SPACER,LED,NYLON,STRIP	5100079-00	2
		SPACER,LED,5-1,.350,15 STATION	5100105-00	0.133
		SPACER,LED ALIGNMENT	5100084-00	1
		PCB SCHEMATIC DIAGRAM	5500140-00 F	REF.

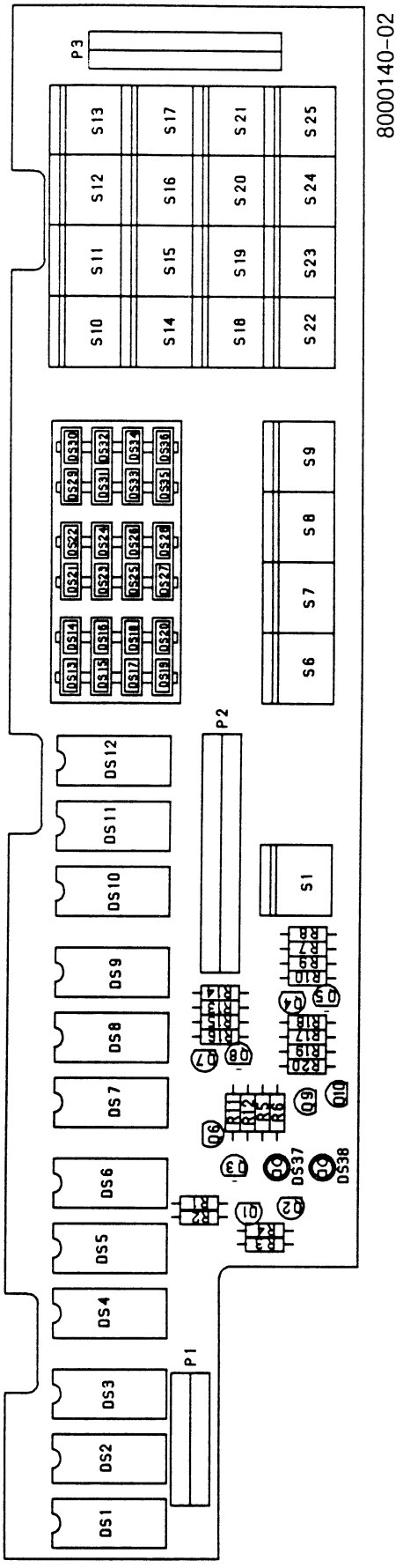
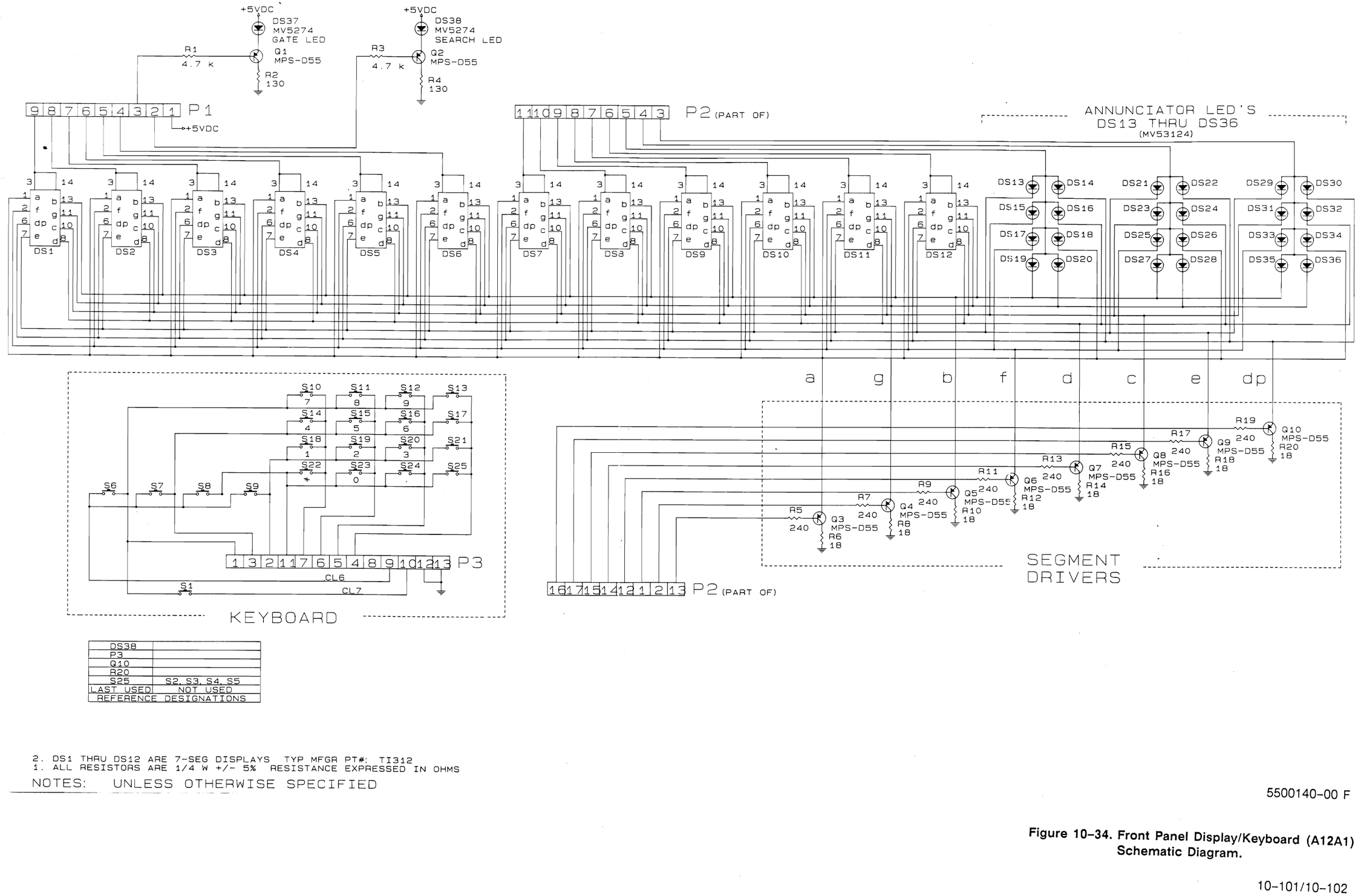


Figure 10-33. Front Panel Display/Keyboard (A12A1) Component Locator.



DS38	
P3	
Q10	
R20	
S25	S2, S3, S4, S5
LAST USED	NOT USED

REFERENCE DESIGNATIONS

2. DS1 THRU DS12 ARE 7-SEG DISPLAYS TYP MFGR PT#: TI312
1. ALL RESISTORS ARE 1/4 W +/- 5% RESISTANCE EXPRESSED IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

5500140-00 F

Figure 10-34. Front Panel Display/Keyboard (A12A1) Schematic Diagram.

A12A2
FRONT PANEL LOGIC
(2020191-01)

The front panel logic assembly contains logic circuitry for control of two functions:

- Display control
- Keyboard control

The +5 V power supply to the front panel assemblies is regulated by a voltage regulator located behind the front panel logic board. For heat-sinking purposes, this voltage regulator is mounted on the chassis.

DISPLAY CONTROL

The signals input to the twelve 7-segment LEDs and the three groups of annunciator lights on the front panel display are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on. The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode, the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by a 4- to 16-line multiplexer (U2), and the appropriate digit driver is turned on. At this time, the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit) turns the segment drivers on the front panel display board on or off.

Display intensity is controlled by varying the duty cycle of the multiplexer. This is done by varying the resistance of potentiometer R4 which, in turn, varies the length of time the decoder U2 and display memories U7, U8 are disabled between each scan clock cycle.

At the start of each gate operation, the GATE LED control is triggered, and the GATE LED lights for the length of the gate time.

MEMORY UPDATE MODE

In this mode, display SCAN/$\overline{\text{UPDATE}}$ control line PA4 (U11 pin 6) is set to logic 0, disabling the multiplexer. The microprocessor-controlled $\overline{\text{clock}}$ PA1 (U11 pin 3) is used to clock display counter (U6).

The microprocessor sets CLEAR/LOAD control line PA5 (U11 pin 7) to logic 1 and triggers the clock input of U6, which clears the display counter and updates display memory U7 and U8. Update mode timing is illustrated in Figure 10-40.

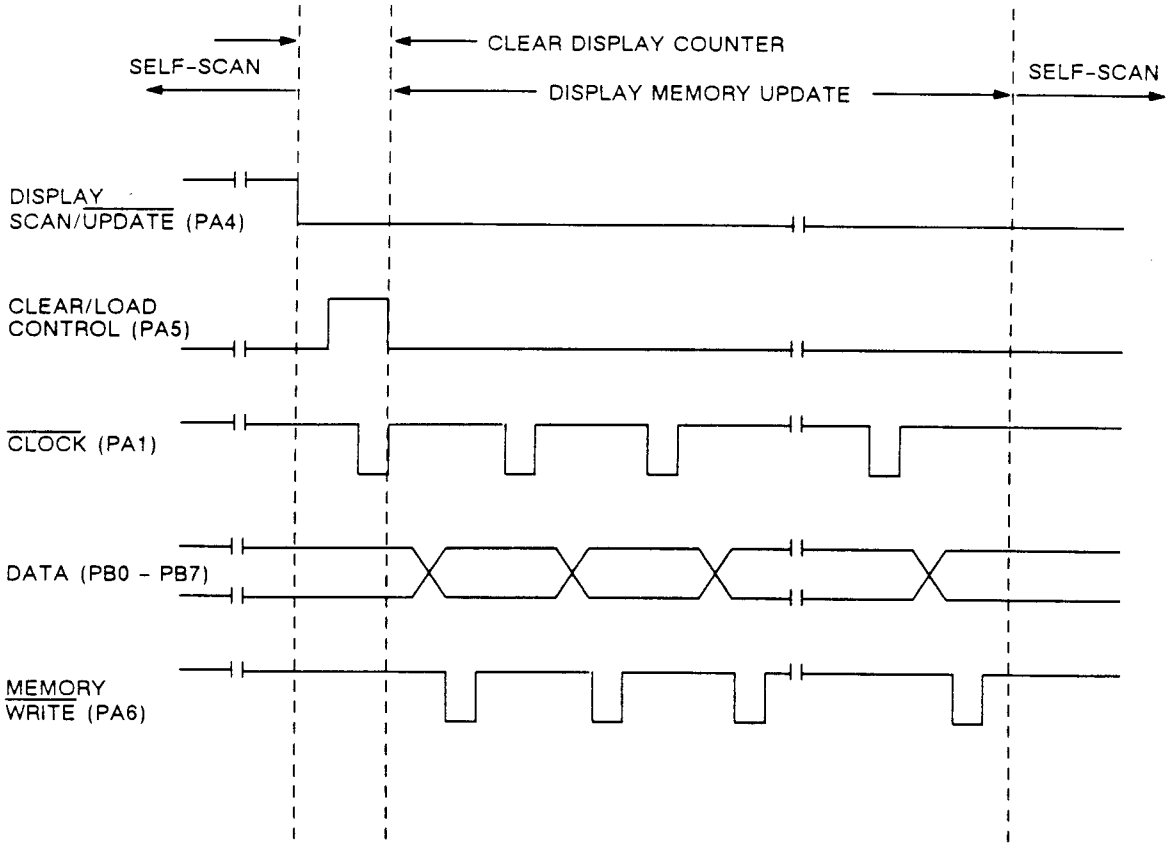


Figure 10-35. Memory Update Mode Sequence.

KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, keyboard READ/$\overline{\text{SCAN}}$ control line PA0 (U11 pin 2) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pressed, all the inputs to 8-input NAND gate U13 are at logic 1 level. When a key is pressed, the column containing that key is grounded. The output of U13 goes to logic 1 and C7 (in the debounce circuit) starts to discharge. When the voltage across C7 reaches approximately +0.7 V above ground, the debounce circuit triggers the interrupt input of the PIA (U11 pin 18), indicating that a key is being pressed.

READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 signal is put on the keyboard READ/$\overline{\text{SCAN}}$ control line PA0 (U11 pin 2). This enables data buffer U9. A 0111 is then loaded into shift register U3 by putting a logic 1 on the clear/load control line PA5 (U11 pin 7) and triggering the clock input of U3. The logic 0 at the output of the shift register U3 is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the four outputs of U3 to determine the coordinate of the key pressed. After the keyboard is read, the keyboard read/scan line is returned to logic 0.

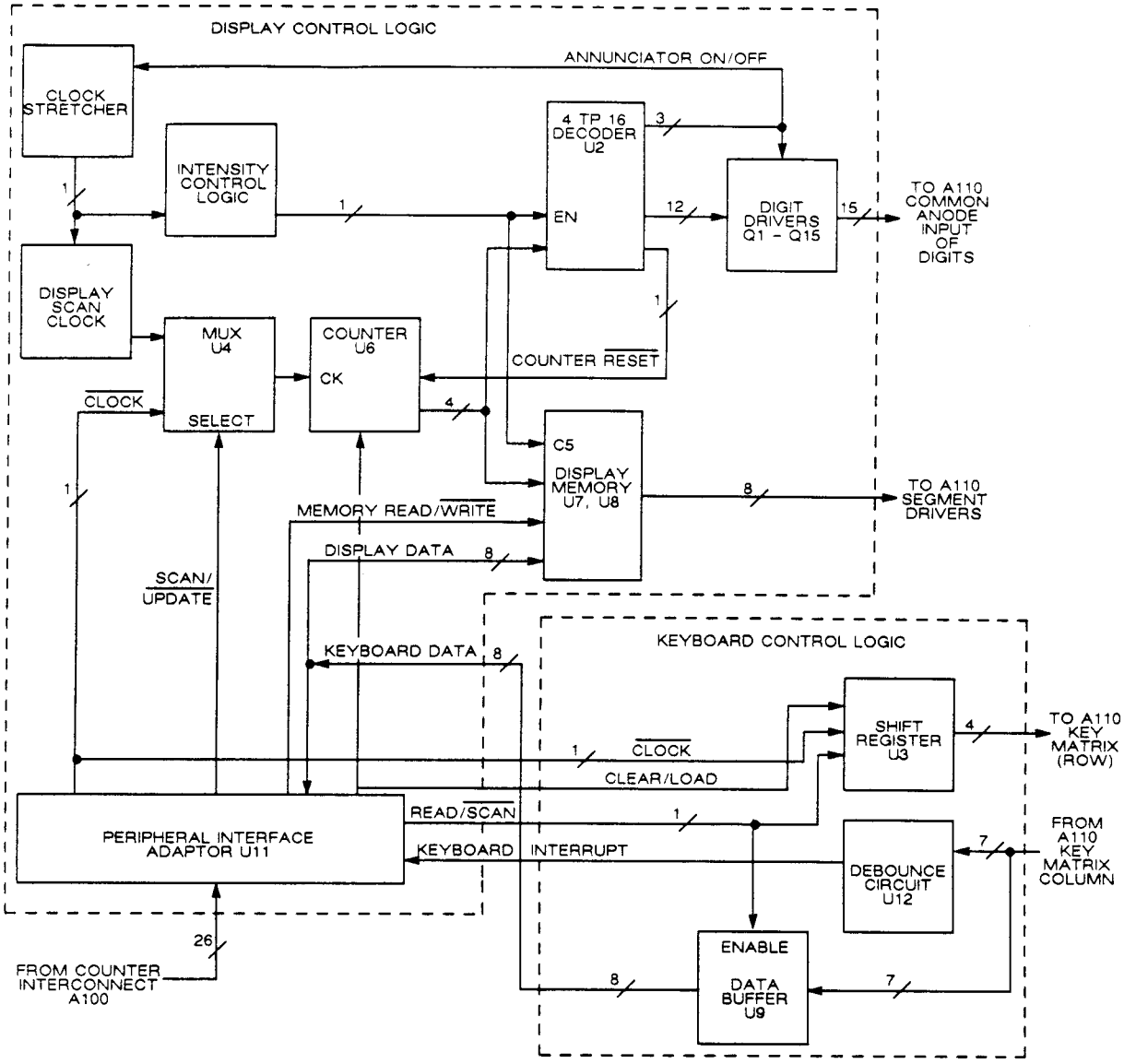


Figure 10-36. Front Panel Logic Functional Block Diagram.

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A12A2 FRONT PANEL LOGIC — 2020191-01 Rev. L

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,TANTALUM	.1µF		35V	2300020-00	1
C2		CAP,DISC,CER	.002µF	20%	1KV	2150005-00	2
C3	C2						
C4		NOT USED					
C5		CAP,TANTALUM	47µF		16V	2300025-00	1
C6		CAP,TANTALUM	2.2µF	20%	16V	2300012-00	1
C7		CAP,TANTALUM	22µF	20%	16V	2300030-00	1
C8		CAP,TANTALUM	.33µF	20%	35V	2300031-00	1
C9		CAP,TANTALUM	33µF		10V	2300015-00	1
C10		CAP,CER	.01µF	20%	100V	2150003-00	6
C11	C10						
C12	C10						
C13	C10						
C14	C10						
C15	C10						
CR1		DIODE,1N4148,FAST SWITCHING,GP				2704148-00	1
J1		CONN,PCB,PLUG,9 PIN				2620062-00	1
J2		CONN,PCB,PLUG,17 PIN				2620064-00	1
J3		CONN,PCB,PLUG,13 PIN				2620063-00	1
J4		CONN,FRICT LK .100,4 PIN				2620068-00	1
J5		CONN,FRICT LK .100,3 PIN				2620121-00	1
P1		NOT USED					
P2		CONN,PCB,RT ANGLE,26 PIN				2620131-00	1
Q1		XSTR,MPSD54,PNP,DARLINGTON				4710027-00	15
Q2	Q1						
Q3	Q1						
Q4	Q1						
Q5	Q1						
Q6	Q1						
Q7	Q1						
Q8	Q1						
Q9	Q1						
Q10	Q1						
Q11	Q1						
Q12	Q1						
Q13	Q1						
Q14	Q1						
Q15	Q1						
Q16		XSTR,2N4124,NPN,GP				4704124-00	2
Q17	Q16						
R1		RES,CC	10K	1/4W	5%	4010103-00	2
R2		RES,CC	220	1/4W	5%	4010221-00	1
R3		RES,CC	75K	1/4W	5%	4010753-00	1
R4		POT,CERMET	200	KT05	0.5W	4250022-00	1
R5		RES,CC	120K	1/4W	5%	4010124-00	1
R6		RES,CC	2.4K	1/4W	5%	4010242-00	1
R7		RES,CC	1K	1/4W	5%	4010102-00	15
R8	R7						
R9	R7						
R10	R7						
R11	R7						
R12	R7						
R13	R7						
R14	R7						
R15	R7						

A12A2 FRONT PANEL LOGIC (Continued) 2020191-01 Rev. L

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R16	R7						
R17	R7						
R18	R7						
R19	R7						
R20	R7						
R21	R7						
R22		NOT USED					
R23		RES,CC	15K	1/4W	5%	4010153-00	1
R24		RES,CC	390	1/4W	5%	4010391-00	1
R25		RES,CC	200	1/4W	5%	4010201-00	1
R26	R7	SEE NOTE 1					
R27	R1						
R28		NOT USED					
R29		RES,CC	2.2K	1/4W	5%	4010222-00	1
R30		NOT USED					
R31		RES,CC	27K	1/4W	5%	4010273-00	1
R32		RES,CC	39K	1/4W	5%	4010393-00	3
R33	R32						
R34	R32						
RN1		RES,NTWK	9X10K	0.2W	2%	4170003-00	2
RN2	RN1						
RN3		RES,NTWK	7X10K	0.3W	2%	4170004-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	9
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
TP6	TP1						
TP7		NOT USED					
TP8	TP1						
TP9	TP1						
TP10	TP1						
U1		IC,74LS123				3084123-00	2
U2		IC,74154				3074154-00	1
U3		IC,SR,PRL ACCESS,4-BIT,TI ONLY				3084195-01	1
U4		IC,74LS51				3087451-00	1
U5		IC,74LS132				3084132-00	1
U6		IC,74LS163				3084163-00	1
U7		IC,74LS189				3057489-00	2
U8	U7						
U9		IC,74LS244				3084244-00	1
U10	U1						
U11		IC,6820,PERIPHERAL INTFC ADAPTER				3086820-00	1
U12		IC,74LS14				3087414-00	1
U13		IC,74LS30				3087430-00	1
XU2		CONN,SOCKET,DIP,24 PIN				2630020-00	1
XU3		CONN,SOCKET,DIP,16 PIN				2630016-00	1
XU11		CONN,SOCKET,DIP,40 PIN				2630022-00	1
HARDWARE USED IN THIS ASSEMBLY							
		STANDOFF,RND (5/32),.140 I.D.X3/16L				5100045-00	9
		PCB SCHEMATIC DIAGRAM				5500191-00 F	REF.

NOTE 1 - R26 SAT AS FOLLOWS: 820 MIN-1.2K MAX

ASSEMBLY CHANGE INFORMATION

This manual may cover multiple instrument CCNs. The following chart provides information on changes that have occurred to this assembly.

Assembly Part Number	CCN Level	Comments
2020191-01	585B: 6804 thru 6806 588B: 6905 thru 6908	Starting assembly.
2020191-02	585B: 6806 588B: 6908	U11 was changed to: IC,68B21P,PRPHL INTERFACE ADAPTER 3086821-00

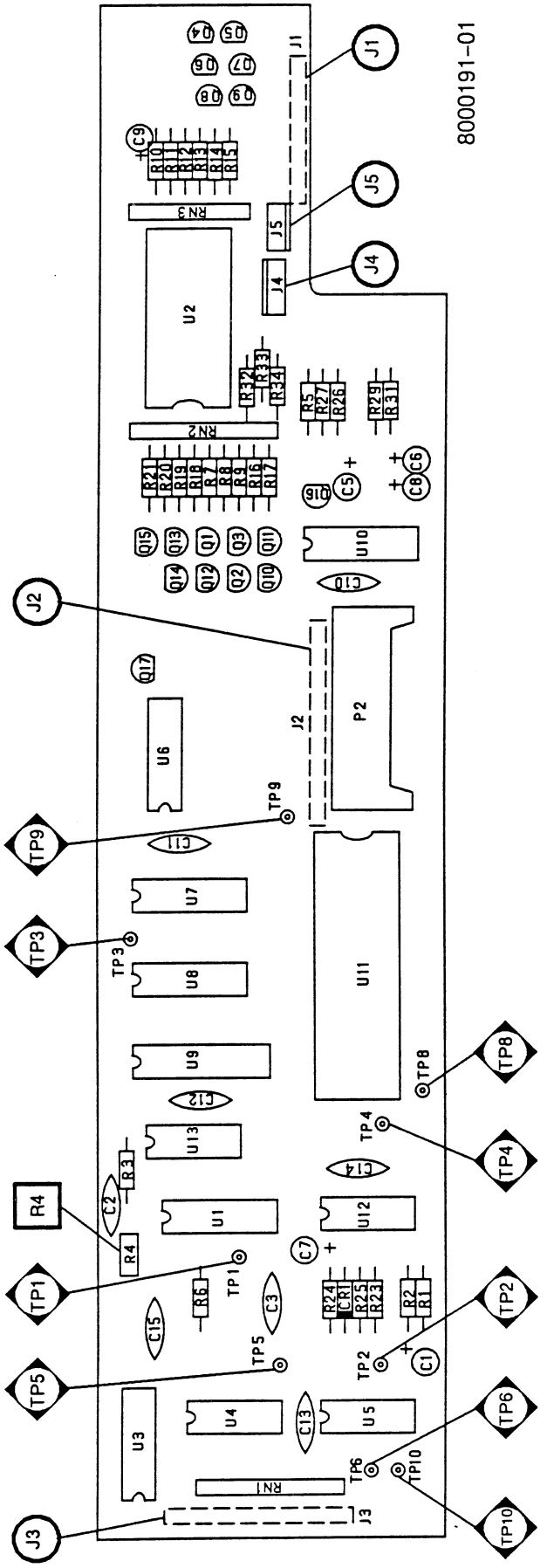
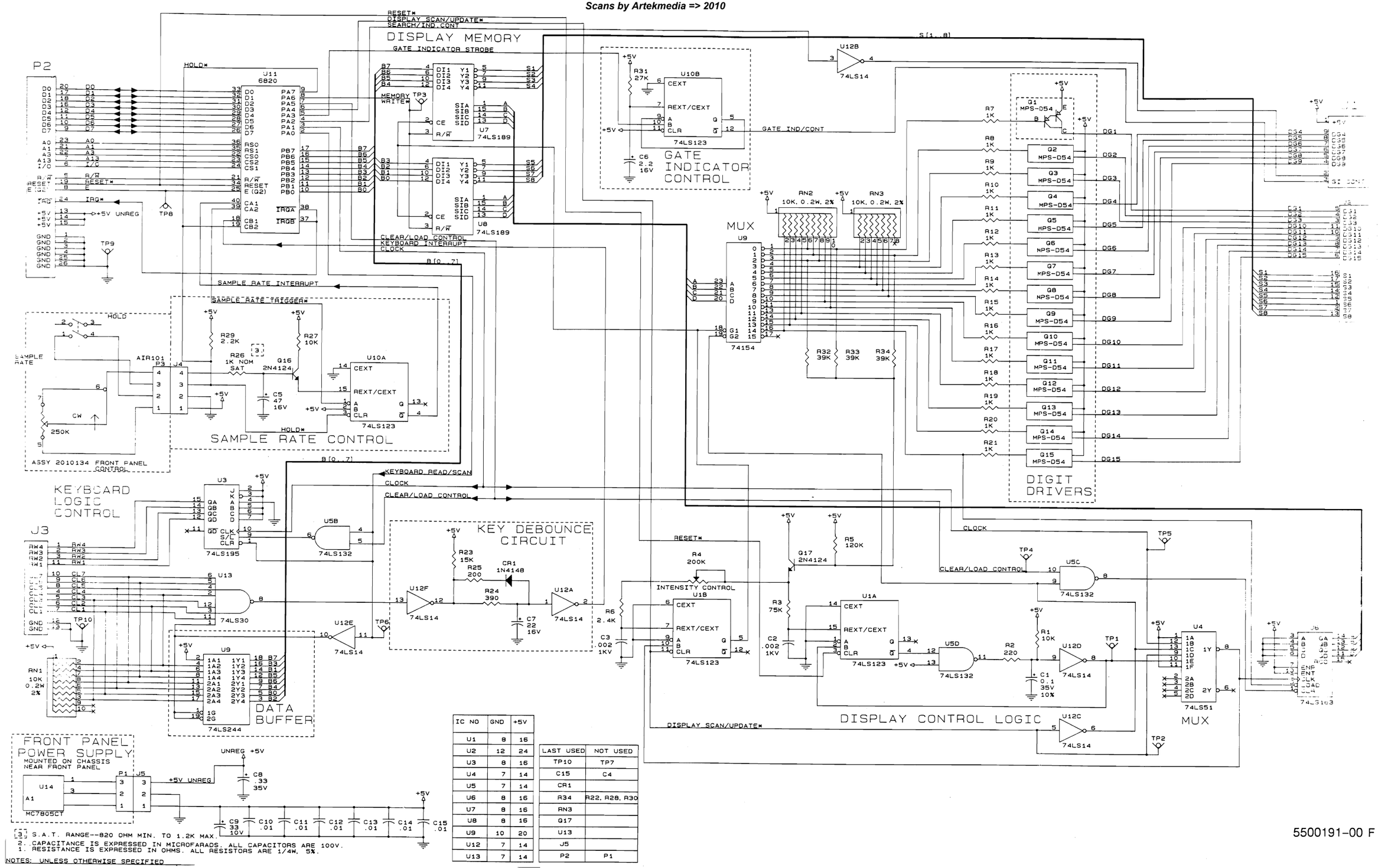


Figure 10-37. Front Panel Logic (A12A2) Component Locator.



IC NO	GND	+5V
U1	8	16
U2	12	24
U3	8	16
U4	7	14
U5	7	14
U6	8	16
U7	8	16
U8	8	16
U9	10	20
U12	7	14
U13	7	14

LAST USED	NOT USED
TP10	TP7
C15	C4
CR1	
R34	R22, R28, R30
RN3	
Q17	
U13	
J5	
P2	P1

5500191-00 F

Figure 10-38. Front Panel Logic (A12A2) Schematic Diagram.

A13
REAR PANEL
2010763-02

The rear panel provides the primary mounting surface for the counter AC power input and voltage select switch, external control (GPIB) interface, and auxiliary signal inputs and outputs. The panel contains the following:

- Rear panel
- Voltage select switch assembly
- Signal input and output coax assemblies
- Fuse assembly
- AC power receptacle
- Fan assembly
- GPIB connector

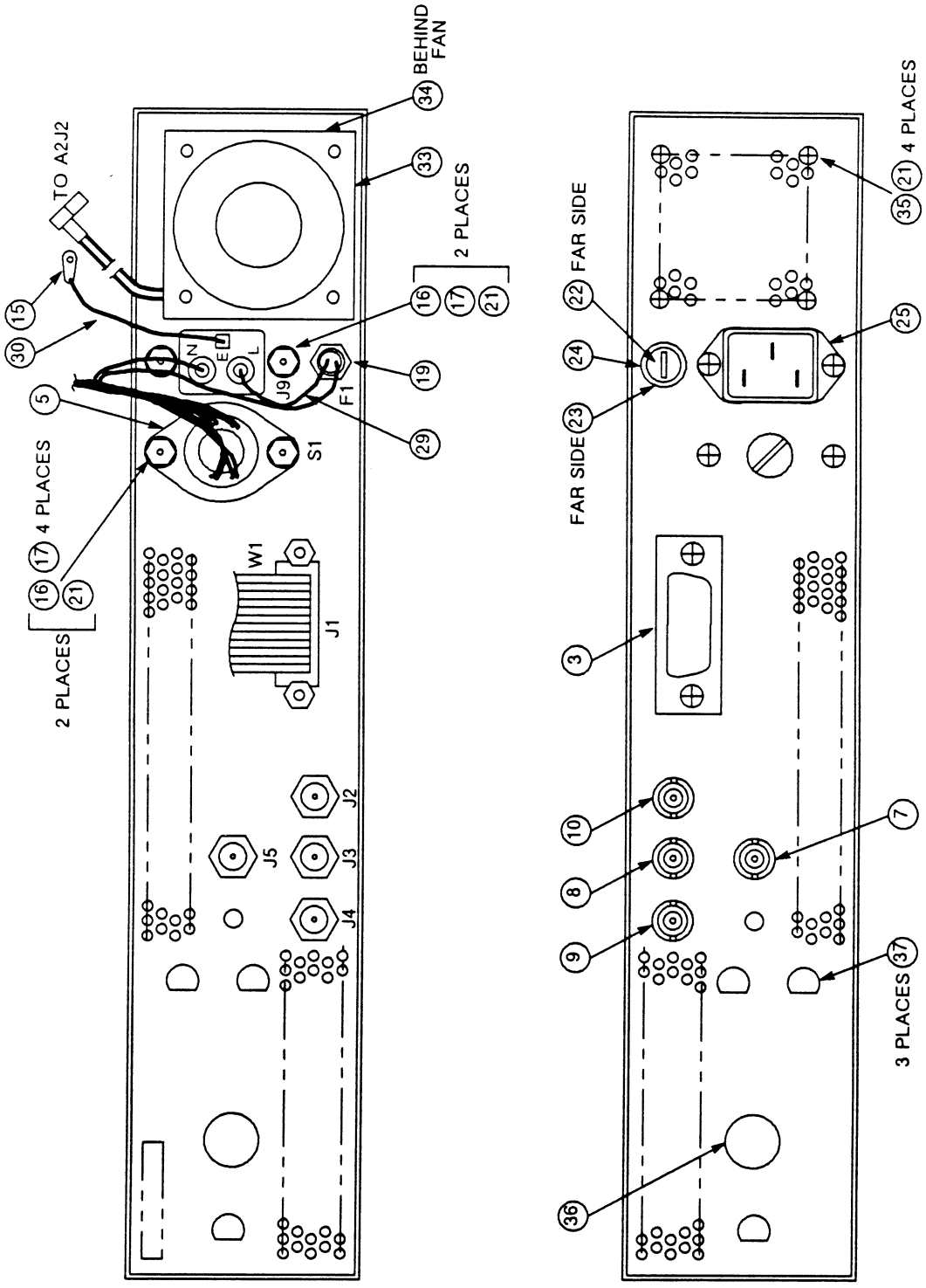


Figure 10-39. Rear Panel (A13).

A13 REAR PANEL 2010763-02 Rev. A

ITEM NO.	DESCRIPTION	EIP NO.	UNITS PER ASSY
1	PANEL,REAR	5210816-02	1
3	CABLE,FLAT RBN,GPIB	2040190-03	1
5	SWITCH ASSY,VOLT SELECT	2040441-01	1
7	COAX ASSY,10MHZ I/O	2040264-01	1
8	CABLE ASSY,COAX,A13W3	2040449-01	1
9	CABLE ASSY,COAX,A13W4	2040450-01	1
10	CABLE ASSY,COAX,A13W2	2040448-01	1
15	SOLDER LUG,#4	5000049-01	1
16	SCR,PNH X-REC 4-40X3/8 UNC	5120004-06	4
17	WASHER,FLAT,CRES NO.4	5160004-00	6
19	WASHER,FIBER	5000192-00	1
21	NUT,HEX,SLFLKG,CRES 4-40 UNC-3B	5184004-40	8
22	FUSE,1.5AMP SB 3AG 250V	5000101-00	1
23	CARRIER,FUSE,3AG,GREY(DOM)	5000171-00	1
24	HOLDER,FUSE,W/MTG NUT	5000170-00	1
25	CONN,RCPT,PWR,W/FILTER	2650005-00	1
29	WIRE,INSUL,18AWG GRY	5418888-00	6
30	WIRE,INSUL,18AWG GRN	5418555-00	3.5 IN.
31	TUBING,SHRINK,3/16 BLK	5480011-00	1
32	TUBING,SHRINK,3/4 BLK	5480005-00	1.5 IN.
33	FAN ASSY, 24VDC	2010723-01	1
34	BRACKET,SPACER,FAN	5210833-01	1
35	SCR,PNH X-REC 4-40X5/8 UNC	5120004-10	4
36	PLUG,METAL,3/4 HOLE DIA	5000206-00	1
37	BUTTON,PLUG .350 ID	5000246-00	3

SECTION11
OPTIONS

This section provides descriptions, specifications, schematic diagrams, and component locators for the following options available for use with the EIP 585B or 588B counter.

Option	Description
5803	Rear Panel Input Connectors
5804	Band 3 Frequency Extension Module. Available on Model 588B only. Required for frequencies between 26.5 GHz and 170 GHz. Frequency Extension Cable Kit 890 and appropriate remote sensors are also required.
5806	2-Year Extended Warranty①
5807	Ovenized High Stability Timebase (aging Rate: 5 x 10^{-9}/day)②
5808	Ovenized High Stability Timebase (aging Rate: 1 x 10^{-9}/day)②
5809	AT-cut Ovenized High Stability Timebase (aging Rate: 5 x 10^{-10}/day)②
5809	SC-cut Ovenized High Stability Timebase (aging Rate: 5 x 10^{-10}/day)

① A three year warranty became standard as of October 1, 1992.

② Options 5807, 5808, and 5809 were discontinued as of December 1992. These discontinued high stability ovenized oscillators incorporated an AT-cut crystal. They were replaced by a new Option 5809 incorporating a SC-cut crystal. The new option 5809 has virtually identical specifications as the old Option 5809, but requires less warm-up time.

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OPTION 5804
EXTENDED FREQUENCY CAPABILITY
(2010807-01) CCN 6905
(2010807-02) CCN 6906, 6907, 6908

THEORY OF OPERATION

NOTE

Because of the extensive test equipment and special processes required to test and repair this assembly, it is not recommended that any field repair be attempted. For this reason, the manual does not contain detailed information on the circuitry contained in this assembly. Exchange modules are available from EIP. Please consult the factory for pricing.

The Band 3 millimeter wave converter is a heterodyne harmonic downconverter that uses millimeter wave harmonic mixers in the various waveguide bands from 26.5 to 170 GHz. These mixers are external to the counter.

When the 588B counter measures a signal frequency greater than 26.5 GHz, using a Model 890 cable and a remote sensor, it downconverts the signal to approximately 675 MHz, where it is directly counted by the Band 2 RF converter. The VCO signal (between 435 and 505 MHz) is multiplied by 12 to the 5.22 to 6.06 GHz range. This signal provides the LO power which is sent through a diplexer to the remote sensor. The remote sensor is a harmonic mixer that generates harmonics of the LO. One of these harmonics mixes with the input to provide an IF at 675 MHz. The IF returns on the same line as the LO and is amplified by a variable gain amplifier to approximately -5 dBm. (See Figure 11-1.) This IF signal is routed to the count chain via the signal conditioner assembly, where it is also prescaled by a factor of four.

Initially the counter determines the sweep range limits of the LO based on the entered subband. The higher the subband number, the smaller the LO sweep range. Then, the LO is swept between its sweep limits and searches for a signal. When a signal is found, the LO is stepped a small amount and, depending on the direction of the IF step, the mix side is found. In the normal mode, the counter uses an 8-point algorithm to determine the LO harmonic number from the ratio of the IF step to the LO step. In the center frequency mode, the harmonic number is calculated based on the entered center frequency. The LO is then adjusted to set the IF to approximately 675 MHz. After each LO step, the IF gain is adjusted to set the detector threshold 3 dB below the peak amplitude.

The IF is measured and the frequency calculated and displayed using the formula:

$$FREQ = N(LO) \pm IF$$

After each measurement, the IF is readjusted to 675 MHz, and the IF gain is readjusted to set the peak 3 dB above threshold. Figure 11-2 is a block diagram of the millimeter wave converter.

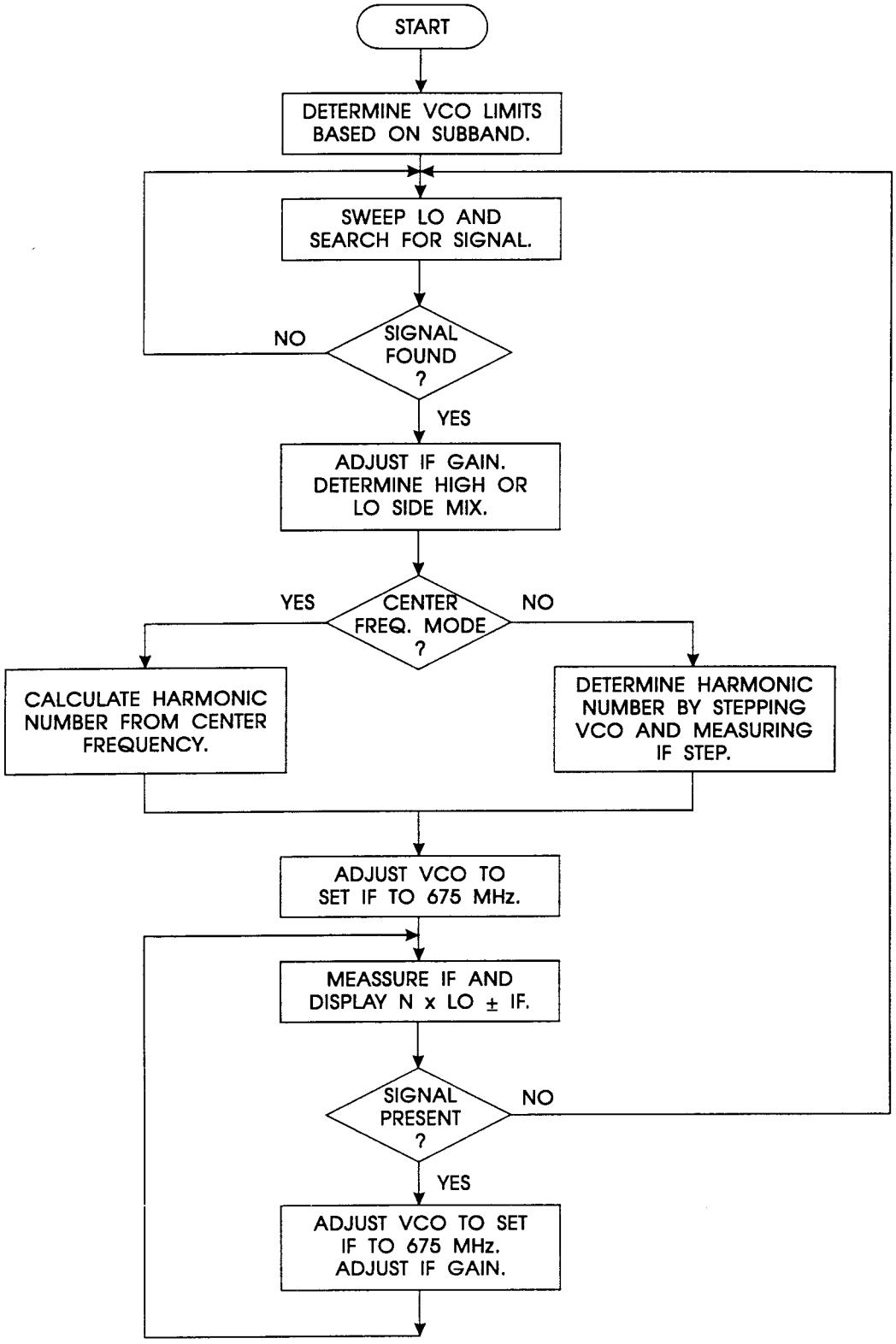

Figure 11-1. Millimeter Wave Converter Lock Process Flow Diagram.

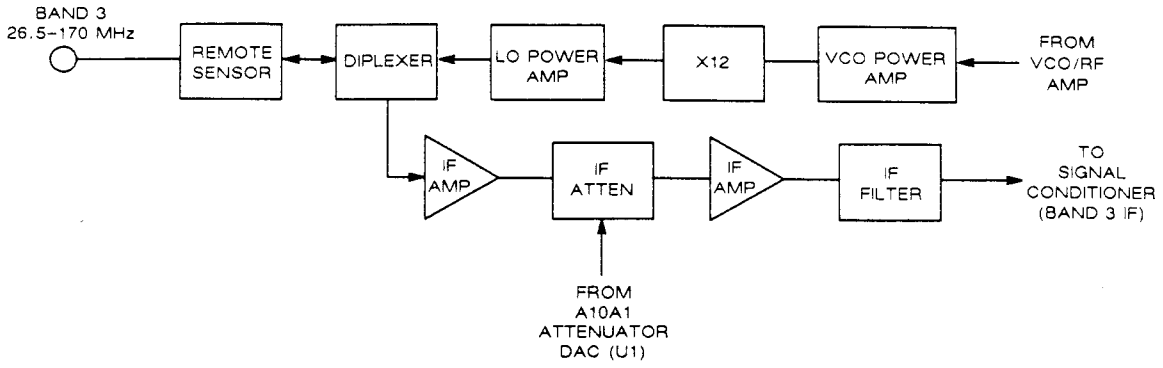

Figure 11-2. Millimeter Wave Converter Block Diagram.

The major components of the converter are:

- Power amplifier
- Multiplier
- IF amplifier

POWER AMPLIFIER

The power amplifier consists of three bipolar transistor stages preceded by a high-pass filter to cut down on wideband noise entering the amplifier. The first stage is operated linearly (class A), and does not require tuning. The second and third stages are turned on by the RF power and must be adjusted for best performance.

MULTIPLIER

The multiplier, consisting of a X3 multiplier, a X4 multiplier, and an LO amplifier diplexer, multiplies the incoming VCO frequency by 12 to supply the LO power to an external mixer. The LO amplifier doubles the output power while providing buffering between the mixer and the multiplier chain. The IF signal, separated in the diplexer, is amplified and filtered in the variable gain IF amplifier strip.

IF AMPLIFIER

The IF amplifier increases the amplitude of the IF signal generated by a harmonic mixer to approximately -5 dBm while suppressing all other signals, such as harmonics of the VCO, present at the input at levels far exceeding that of the desired IF signal. Since the amplifier processes pulsed signals, it must always be kept in the linear operating range, regardless of the IF input level. This is done by varying the bias current of two of the amplifier stages by microprocessor control, according to output level, to keep the output level constant at approximately -5 dBm.

CALIBRATION

The calibration procedure described below should be used to calibrate the Extended Frequency Capability option. The recommended calibration interval is six months. Further calibration within this time interval should be made if the counter does not operate as specified, or if it has been repaired. If the adjustments do not result in the specified performance, refer to the troubleshooting section.

GATE ERROR CALIBRATION

Gate Error Calibration Performance Specifications.

Function	Performance Specification	Method
Gate error calibration	Gate error ≤ ±0.03/GW	Use Special Function 92 to calibrate gate accuracy

Equipment Required

Minimum use specifications are the principal parameters required for calibration and are included to assist in selecting alternative equipment. Satisfactory performance of alternative equipment should be verified prior to use. All applicable equipment must bear evidence of current calibration.

Table 11-1. Calibration Equipment Required.

Description	Critical Parameter	Recommended Manufacturer	Model
Pulse generator	20 ns pulses	Wavetek	801
50 ohm feedthrough termination	50 ohms resistance	Pamona	4119-50
Oscilloscope	100 MHz bandwidth	Tektronix	475
Frequency extender	26.5 - 60 GHz	Watkins Johnson	1204-42
Synthesized sweeper	250 MHz to 26.5 GHz	HP	8340B
Remote sensor	26.5 to 40 GHz	EIP	091
Cable kit		EIP	890

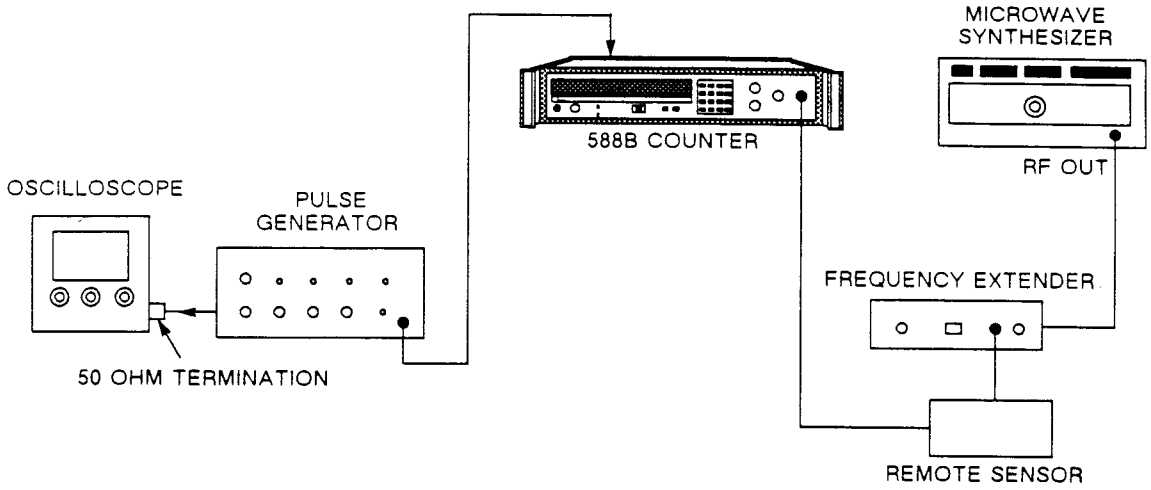

Figure 11-3. Gate Error Calibration Setup.

Procedure

1. Set up equipment as shown in Figure 11-3 and described below.

2. Using the appropriate remote sensor, apply a CW signal to the BAND 3 input connector.

NOTE

Band 3 need not be calibrated for every subband. Calibration of any subband is sufficient for all of Band 3.

3. Select Band 3 and the appropriate subband.

4. Connect the pulse generator to the oscilloscope through a 50 ohm termination at the oscilloscope. Set the pulse generator as follows:

   PRF: 1 MHz
   Complementary pulse width: 50 ns
   Base line: 0 V
   Amplitude: -1 V

   Connect the pulse generator to the INHIBIT IN connector on the rear panel of the counter.

5. Press keys for Special Function 92, then press TRIG key. The counter remains in the autocalibrate state for about three minutes.

PERFORMANCE VERIFICATION TESTS

Following are the performance verification test procedures for the Extended Frequency Capability option. These procedures are summarized in Table 11-2.

Table 11-2. Performance Verification Test Methods.

Counter Characteristic	Performance Specifications	Test Method
Frequency Range		
Minimum Frequency	Band 3-1: 26.5 GHz Band 3-2: 33 GHz Band 3-3: 40 GHz Band 3-4: 50 GHz Band 3-5: 60 GHz Band 3-6: 75 GHz Band 3-7: 90 GHz Band 3-8: 110 GHz	Checked by verifying that counter displays accurate reading of frequency input from millimeter wave sources (see Special Equipment Section).
Maximum Frequency	Band 3-1: 40 GHz Band 3-2: 50 GHz Band 3-3: 60 GHz Band 3-4: 75 GHz Band 3-5: 90 GHz Band 3-6: 110 GHz Band 3-7: 140 GHz Band 3-8: 170 GHz	Checked by verifying that counter displays accurate reading of frequency input from millimeter wave sources (see Special Equipment Section).
Sensitivity		
26.5 to 60 GHz 60 to 170 GHz (Model 588B)	-20 dBm -15 dBm	Checked by verifying that the counter displays a reading within 1 kHz of signal input from signal generator at specified power level.
Maximum Input		
26.5 to 170 GHz (Model 588B)	+5 dBm	Checked by verifying that the counter displays a measurement within ±1 kHz of input signal at maximum power level.
Amplitude Discrimination		
26.5 to 170 GHz (Model 588B)	20 dB	Checked by verifying that the counter measures the higher power signal of the signals input from signal generators.
Gate Error		
26.5 to 170 GHz (Model 588B)	Gate Error (in Hz) = ±0.03/ Gate Width	Checked by verifying that the counter displays measurement within the limits of the gate error when appropriate inhibit input and signal are applied.

Table 11-2. Performance Verification Test Methods. (Continued)

Counter Characteristic	Performance Specifications	Test Method
Distortion Error		
26.5 to 170 GHz (Model 588B)	Distortion Error (in Hz) = ± 0.01/ Pulse Width (in Seconds) - 3×10^{-8}	Checked by calculating the distortion error by subtracting the gate error from the frequency of a pulsed signal input from a signal generator and verifying that it falls within the specification.
Averaging Error		
26.5 GHz to 170 GHz (Model 588B)	Averaging Error = $\pm(2)\sqrt{[RES / (GW)(AVG)^*}$	Checked by using the displayed frequency of a number of measured pulsed signals input from a signal generator to calculate the sample variance and then verifying that it is within the specified limits.

*RES is the specified instrument resolution in Hz (This is true up to 1 MHz resolution. Above 1 MHz resolution RES = 10^6 Hz.) GW in seconds is the logical AND of inhibit and pulse width minus 3×10^{-8} seconds. AVG is the number of specified count average.

EQUIPMENT REQUIREMENTS

Equipment required for testing the millimeter wave converter is listed in Table 11-3.

NOTE

Minimum use specifications are the principal parameters required for performance of the procedures and are included to assist in the selection of alternate equipment. Satisfactory performance of alternate items should be verified prior to use. All applicable equipment must bear evidence of current calibration.

Table 11-3. Equipment Required.

Equipment	Range	Recommended Manufacturer	Model
Synthesized sweeper	10 MHz to 26.5 GHz	Hewlett Packard	8340B
Microwave amplifier	2 to 20 GHz	Hewlett Packard	8349B
Power meter	10 MHz to 40 GHz	Hewlett Packard	437B
Power meter	40 to 170 GHz	Hewlett Packard	432A
Power sensor	26.5 to 40 GHz	Hewlett Packard	8486A
Power sensor	40 to 60 GHz	Hughes	4577UH-1000
Power sensor	60 to 90 GHz	Hughes	4577EH-1000

Table 11-3. Equipment Required. (Continued)

Equipment	Range	Recommended Manufacturer	Model
Power sensor	90 to 110 GHz	Hughes	4577WH-1400/100
Power sensor	110 to 170 GHz	Hughes	45778H-1X00
Gunn diode oscillator	94 GHz	Millitech	GDM-10-4-1
Oscilloscope	DC to 100 MHz	Tektronix	475
Pulse generator	5 Hz to 50 MHz	Wavetek	801
Pulse modulator	2 to 18 GHz	Hewlett Packard	11720A
Remote sensor	26.5 to 170 GHz	EIP	091 through 098
Cable kit		EIP	890
10 dB coupler		Hughes	45326H-1010
Microwave switch	SP5T	Watkins Johnson	MSF503
Microwave attenuator, variable	0 to 25 dB	Hughes	45736H-1200
Frequency extender	X2, X3 X4 X6 X9 X12	Watkins Johnson Millitech Millitech Millitech Millitech	1204-02 FEX-15-1 FEX-10-1 FEX-06-1 FEX-05-1

RANGE/SENSITIVITY TESTS

Description

This test verifies counter operation from 26.5 to 170 GHz at an input power of -20 dBm (-15 dBm from Band 3-4 through Band 3-8).

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Microwave amplifier (Hewlett Packard 8349B)
Microwave switch (Watkins Johnson MSF 503)
Frequency extender x2, x3 (Watkins Johnson 1204-2)
Frequency extender x4 (Millitech FEX-15-1)
Frequency extender x6 (Millitech FEX-10-1)
Frequency extender x9 (Millitech FEX-06-1)
Frequency extender x12 (Millitech FEX-05-1)
Remote sensors (EIP 091 through 098)
Cable kit (EIP 890)
Power meter (Hewlett Packard 437B)
Power meter (Hewlett Packard 432A)
Power sensor (Hewlett Packard 8486A)
Power sensor (Hughes 4577UH-1000)
Power sensor (Hughes 4577EH-1000)
Power sensor (Hughes 4577WH-1400/100)
Power sensor (Hughes 45778H-1X00)

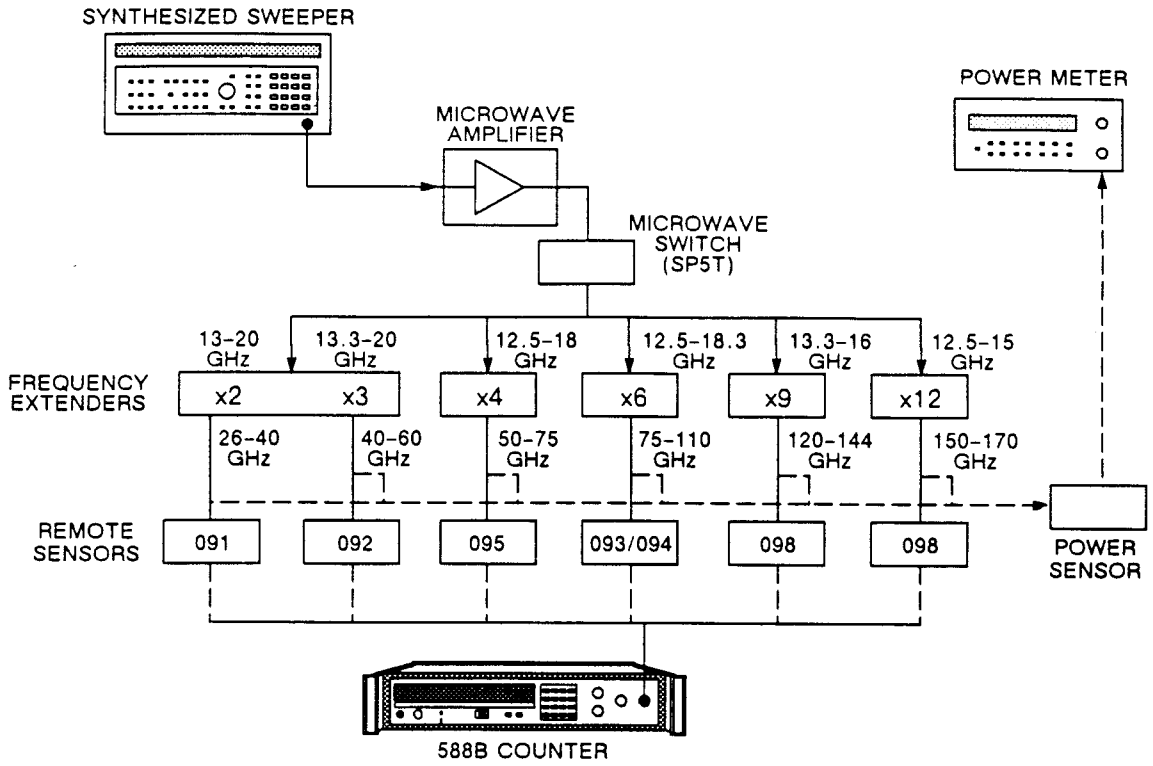

Figure 11-4. Range and Sensitivity Test Setup.

Procedure

1. Connect equipment as shown in Figure 11-4.
2. Set 588B counter to Band 3-1 and select resolution 3.
3. Set output frequency of sweep generator to 13.25 GHz.
4. Using power meter, set output signal level from sweep generator to -20 dBm.
5. Apply 26.5 GHz signal to remote sensor and verify proper reading.

NOTE

In the following steps, set sensitivity to -15 dBm for Bands 3-4 and up.

5. Repeat steps 2, 3, and 4 every 5 GHz up to 170 GHz, changing sources, Band 3 subbands, remote sensors, and power sensors as necessary.
6. Repeat steps 2 through 5 at the input power of +5 dBm.

Table 11-4. Subband Frequency and Power Ranges.

Band	Minimum Frequency (GHz)	Maximum Frequency (GHz)	Minimum Power (dBm)	Maximum Power (dBm)	Damage Power (dBm)
3-1 (Ka)	26.5	40	-20	+5	+10
3-2 (Q)	33	50	-20	+5	+10
3-3 (U)	40	60	-20	+5	+10
3-4 (V)	50	75	-20/-15	+5	+10
3-5 (E)	60	90	-15	+5	+10
3-6 (W)	75	110	-15	+5	+10
3-7 (F)	90	140	-15	+5	+10
3-8 (D)	110	170	-15	+5	+10

AMPLITUDE DISCRIMINATION TEST

Description

This test verifies that the counter will measure accurately the larger of two signals differing in amplitude by 20 dB or more.

CAUTION

Do not exceed maximum specified power when performing this test.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Frequency extender x6 (Millitech FEX-10-1)
10 dB coupler (Hughes 45776H-1400)
Power meter (Hewlett Packard 432A)
Gunn diode oscillator, 94 GHz (Millitech GDM-10-4-17)
Power sensor (Hughes 4577WH-1400/100)
Remote sensor (EIP 095)
Microwave attenuator, variable (Hughes 45736H-1200)

Procedure

1. Connect equipment as shown in Figure 11-5.
2. Set variable attenuator for 16 dB attenuation.
3. Turn on Gunn oscillator and measure output power, after coupler, with the power meter. Adjust variable attenuator for output power of +5 dBm.
4. Measure and record frequency from Gunn oscillator using 588B.
5. Turn off Gunn oscillator.

6. Turn on synthesizer and X6 multiplier.

7. Using the 588B, measure the multiplied frequency from the synthesizer. Set frequency to be 100 MHz away from the Gunn oscillator frequency measured in step 4.

8. Using the power meter, measure output power from coupler and set at -15 dBm.

9. Reconnect signal to 588B and turn on Gunn oscillator. Press reset on counter and verify counter locks on the signal from the Gunn oscillator and measures accurately.

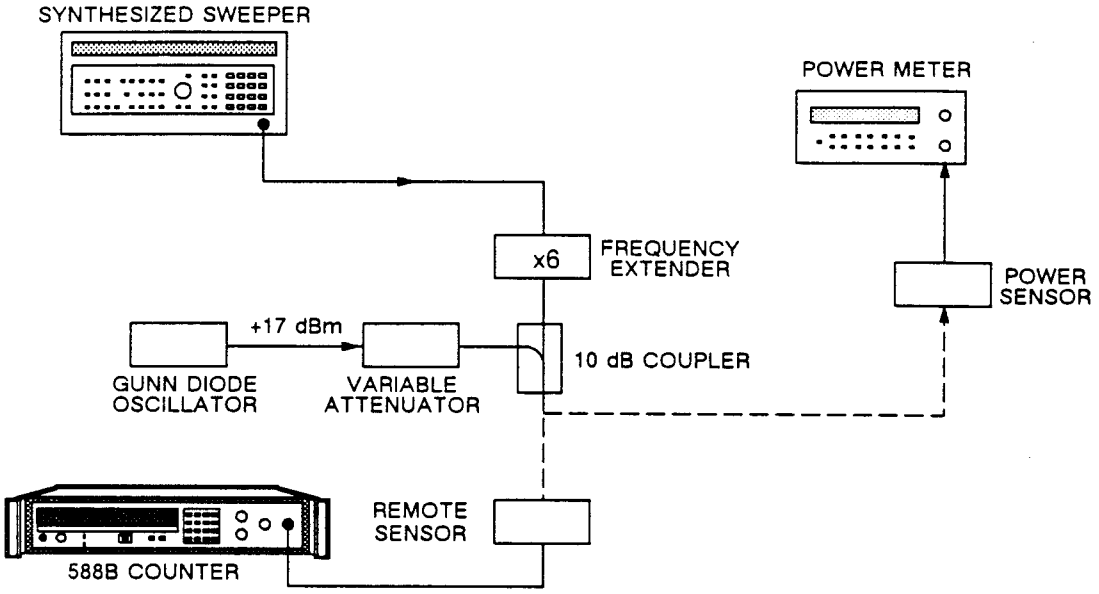

Figure 11-5. Amplitude Discrimination Test Setup.

GATE ERROR TEST

Description

This test verifies that the gate error in Band 3 is within the limits defined by the equation:

$$GE = (\pm 0.03) / (GW)$$

where: GE is the gate error in Hz
GW, in seconds, is the logical AND of inhibit and pulse width minus 30 ns

The measurement is performed with a CW input signal and an inhibit signal.

Equipment Required

Pulse generator (Wavetek 801)
Synthesized sweeper (Hewlett Packard 8340B)
Microwave amplifier (Hewlett Packard 8349B)
Microwave switch (Watkins Johnson MSF 503)
Frequency extender x2, x3 (Watkins Johnson 1204-2)
Frequency extender x4 (Millitech FEX-15-1)
Frequency extender x6 (Millitech FEX-10-1)
Frequency extender x9 (Millitech FEX-06-1)
Frequency extender x12 (Millitech FEX-05-1)
Remote sensor (EIP 091 through 098)

Power meter (Hewlett Packard 437B)
Power meter (Hewlett Packard 432A)
Power sensor (Hewlett Packard 8486A)
Power sensor (Hughes 4577UH-1000)
Power sensor (Hughes 4577EH-1000)
Power sensor (Hughes 4577WH-1400/100)
Power sensor (Hughes 45778H-1X00)
Oscilloscope (Tektronix 475)

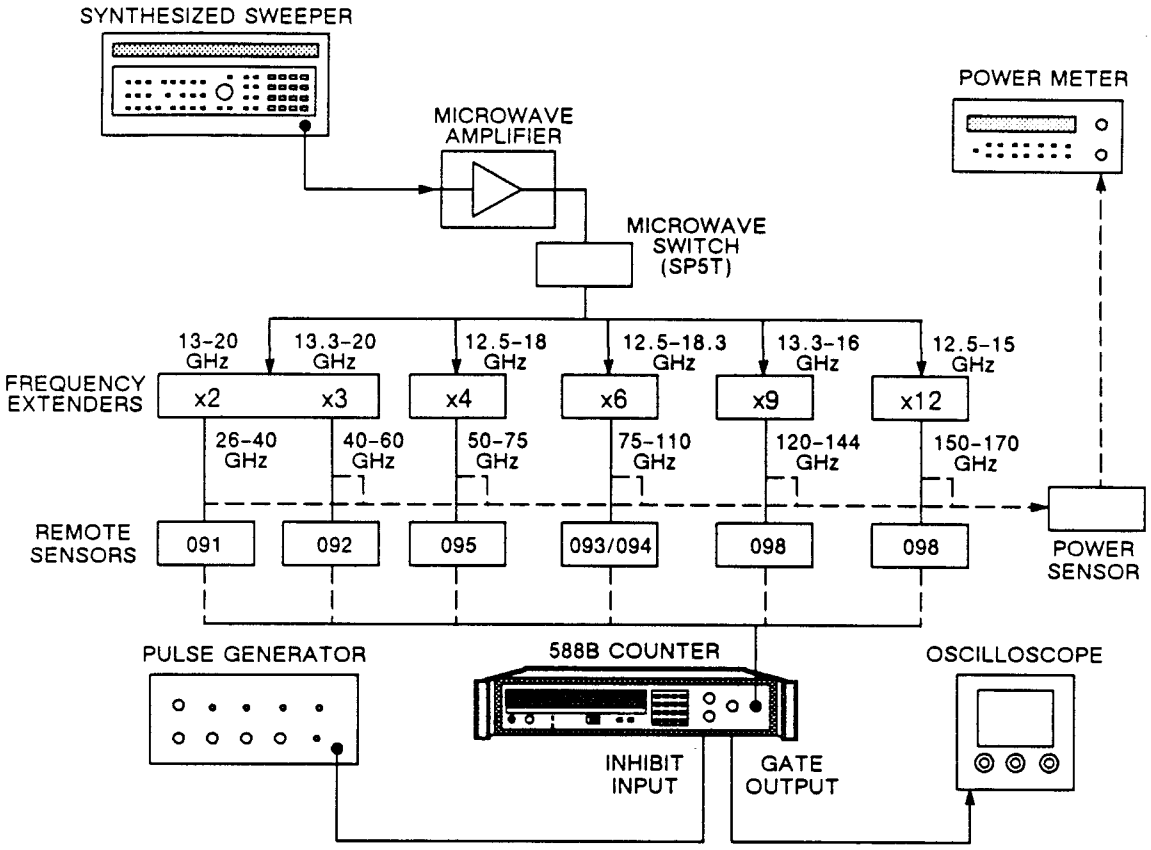

Figure 11-6. Gate Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 11-6 and turn equipment on.
2. Set pulse generator to complimentary mode, 0 to -1 volt pulse amplitude into a 50 ohm load, 1 MHz PRF, and 50 ns pulse width.
3. Set 588B counter to Band 3-1; set averaging feature to 99.
4. Set input frequency to counter to 26.5 GHz, and power to approximately -10 dBm.
5. Connect pulse generator output to inhibit input of counter. Connect gate output from counter to oscilloscope. Adjust inhibit pulse width until gate output pulse width equals 20 ns. Verify that reading on counter is within limits of gate error.
6. Repeat steps 4 and 5 with 100 ns and 1 μs gate width while keeping duty cycle (the ratio of pulse width to pulse period) constant.

7. Repeat measurements at 30 GHz and every 5 GHz to 170 GHz, changing frequency sources, remote sensors, and Band 3 subbands as necessary.

DISTORTION ERROR TEST

Description

This test verifies that the distortion error in Band 3 is within the limits defined by the equation:

$$DE = (\pm 0.03) / (PW - 3 \times 10^{-8})$$

where DE is distortion error in Hz
PW is pulse width in seconds

The measurement is performed by counting the frequency of a pulsed signal and subtracting the gate error from the result.

NOTE

Gate error must be known (see gate error test in this section) before performing this test.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Microwave amplifier (Hewlett Packard 8349B)
Microwave switch (Watkins Johnson MSF 503)
Frequency extender x2, x3 (Watkins Johnson 1204-2)
Frequency extender x4 (Millitech FEX-15-1)
Frequency extender x6 (Millitech FEX-10-1)
Frequency extender x9 (Millitech FEX-06-1)
Frequency extender x12 (Millitech FEX-05-1)
Remote sensor (EIP 091 through 098)
Power meter (Hewlett Packard 437B)
Power meter (Hewlett Packard 432A)
Power sensor (Hewlett Packard 8486A)
Power sensor (Hughes 4577UH-1000)
Power sensor (Hughes 4577EH-1000)
Power sensor (Hughes 4577WH-1400/100)
Power sensor (Hughes 45778H-1X00)
Pulse modulator (Hewlett Packard 11720A)

Procedure

1. Connect equipment as shown in Figure 11-7 and turn equipment on.

2. Set 588B counter to Band 3; set average to 99.

3. Connect signal through remote sensor (using it as a detector) to oscilloscope as shown. Set synthesized sweeper frequency to 26.5 GHz.

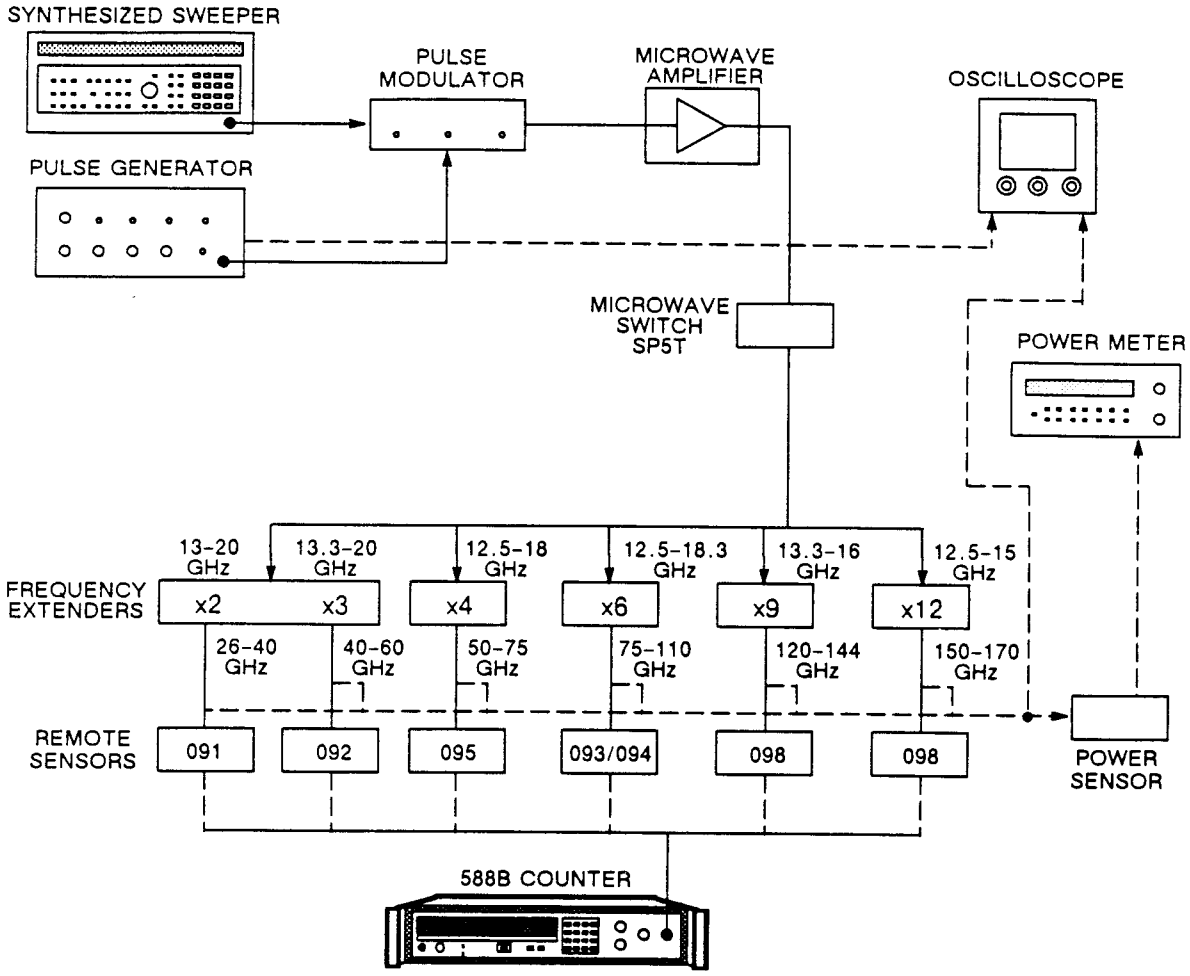

Figure 11-7. Distortion Error Test Setup.

4. Set pulse generator to 1 MHz PRF and 50 ns pulse width at +3.0 to -0.5 volts.

5. Adjust pulse width and voltage levels slightly until pulsed RF signal is 50 ns wide and has a good on/off ratio.

6. Take one measurement.

7. Calculate:

   Distortion Error = (Current Measurement) - (Gate Error)

   Gate error is error measured by gate error test in this section.

8. Verify that distortion error is within specification.

9. Repeat steps 4 to 8 with 100 ns, and 1 μs, pulse width while keeping duty cycle (the ratio of pulse width to pulse period) constant.

10. Repeat steps 4 through 9 every 5 GHz up to 170 GHz, changing sources, remote sensors, and Band 3 subbands as necessary.

AVERAGING ERROR TEST

Description

This test verifies that the averaging jitter in Band 3 is within the limits defined by the equation:

$$AJ = \pm(2)\sqrt{[RES\ /\ (GW)(AVG)]}$$

where AE is the RMS averaging error in Hz.

RES is the specified instrument resolution in Hz. (This is true up to 1 MHz resolution. Above 1 MHz resolution, RES is 1 MHz.)

GW, in seconds, is the logical AND of inhibit and pulse width minus $3x10^{-8}$ seconds.

AVG is the number of specified count average.

The measurement is performed by counting the frequency of n pulsed signals and calculating the standard deviation given as:

$$S = \sqrt{\sum_{i=0}^{i=n-1} (F_i - F_{AVG})^2 / (n-1)} \qquad \text{(standard deviation)}$$

where F_{AVG} is the average frequency measurement minus the gate error and the distortion error and Fi is the current reading.

Equipment Required

Synthesized sweeper (Hewlett Packard 8340B)
Microwave amplifier (Hewlett Packard 8349B)
Microwave switch (Watkins Johnson MSF 503)
Frequency extender x2, x3 (Watkins Johnson 1204-2)
Frequency extender x4 (Millitech FEX-15-1)
Frequency extender x6 (Millitech FEX-10-1)
Frequency extender x9 (Millitech FEX-06-1)
Frequency extender x12 (Millitech FEX-05-1)
Remote sensor (EIP 091 through 098)
Power meter (Hewlett Packard 437B)
Power meter (Hewlett Packard 432A)
Power sensor (Hughes 4577UH-1000)
Power sensor (Hughes 4577EH-1000)
Power sensor (Hughes 4577WH-1400/100)
Power sensor (Hughes 45778H-1X00)

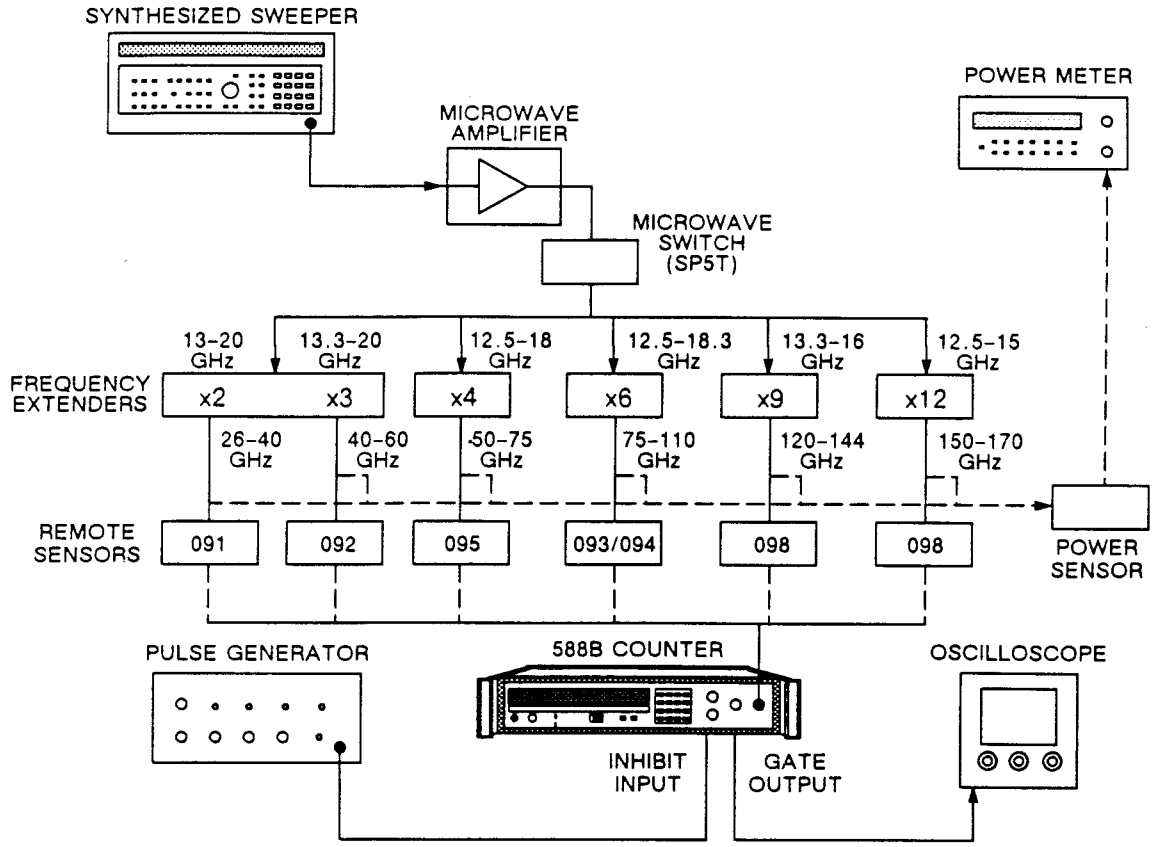

Figure 11-8. Averaging Error Test Setup.

Procedure

1. Connect equipment as shown in Figure 11-8 and turn equipment on.
2. Set pulse generator to complementary mode, 0 volt to -1 volt pulse amplitude into a 50 ohm load, 1 MHz PRF, and 50 ns pulse width.
3. Set 588B counter to Band 3-1; set averaging feature to 99.
4. Set input frequency to counter to 33 GHz and power to approximately -10 dBm. CW reading on counter should be equal to input frequency.
5. Connect pulse generator output to inhibit input of counter. Connect gate output from counter to oscilloscope. Adjust inhibit pulse width until average width is 20 ns.
6. Take one frequency measurement. This reading is FAVG.
7. Turn averaging function off. Turn SAMPLE RATE knob to HOLD.
8. Take 10 measurements by pressing TRIG key 10 times.
9. Calculate:

$$S = \sqrt{\sum_{i=0}^{i=n-1} (F_i - F_{AVG})^2 / (n-1)}$$

10. Calculate:

$$AJ = \pm(2)\sqrt{[RES / (GW)(AVG)]}$$

11. Verify that S < AE.

12. Repeat steps 5 through 11 changing sources as necessary at following frequencies:

Band 3-2	41 GHz	Band 3-6	92 GHz
Band 3-3	50 GHz	Band 3-7	110 GHz
Band 3-4	62 GHz	Band 3-8	150 GHz
Band 3-5	75 GHz		

TROUBLESHOOTING

TROUBLESHOOTING TREE

The troubleshooting tree, shown in Figure 11-10, is intended only as a guide and does not describe every possible failure situation. Turn power off before removing or installing any PC boards or connectors.

Table 11-5. Equipment Required for Troubleshooting.

Equipment	Range	Recommended Manufacturer	Model
Synthesized sweeper	10 MHz to 26.5 GHz	Hewlett Packard	8340B
Microwave amplifier	2 to 20 GHz	Hewlett Packard	8349B
Power meter	10 MHz to 40 GHz	Hewlett Packard	437B
Power meter	40 to 170 GHz	Hewlett Packard	432A
Power sensor	26.5 to 40 GHz	Hewlett Packard	8486A
Power sensor	40 to 60 GHz	Hughes	4577UH-1000
Power sensor	60 to 90 GHz	Hughes	4577EH-1000
Power sensor	90 to 110 GHz	Hughes	4577WH-1400/100
Gunn diode oscillator	94 GHz	Millitech	GDM-10-4-17
Oscilloscope	DC to 100 MHz	Tektronix	475
Pulse generator	5 Hz to 50 MHz	Wavetek	801
Pulse modulator	2 to 18 GHz	Hewlett Packard	11720A
Remote sensor	26.5 to 170 GHz	EIP	091 through 098
Cable kit		EIP	590
10 dB coupler		Hughes	45326H-1010
Microwave switch	SP5T	Watkins Johnson	MSF503
Frequency extender	X2, X3 X4 X6 X9 X12	Watkins Johnson Millitech Millitech Millitech Millitech	1204-02 FEX-15-1 FEX-10-1 FEX-06-1 FEX-05-1

Before servicing any unit, verify that:

1. The line voltage and fuse are correct for the voltage setting.
2. Special Function 09 is selected (internal 10 MHz time base). If Special Function 08 is selected (external 10 MHz time base), check that a proper 10 MHz signal is applied to the 10 MHz IN/OUT connector.
3. The MIN PRF function is properly set. (See Section 3.)
4. The counter is not inhibited by the rear panel INHIBIT IN function.

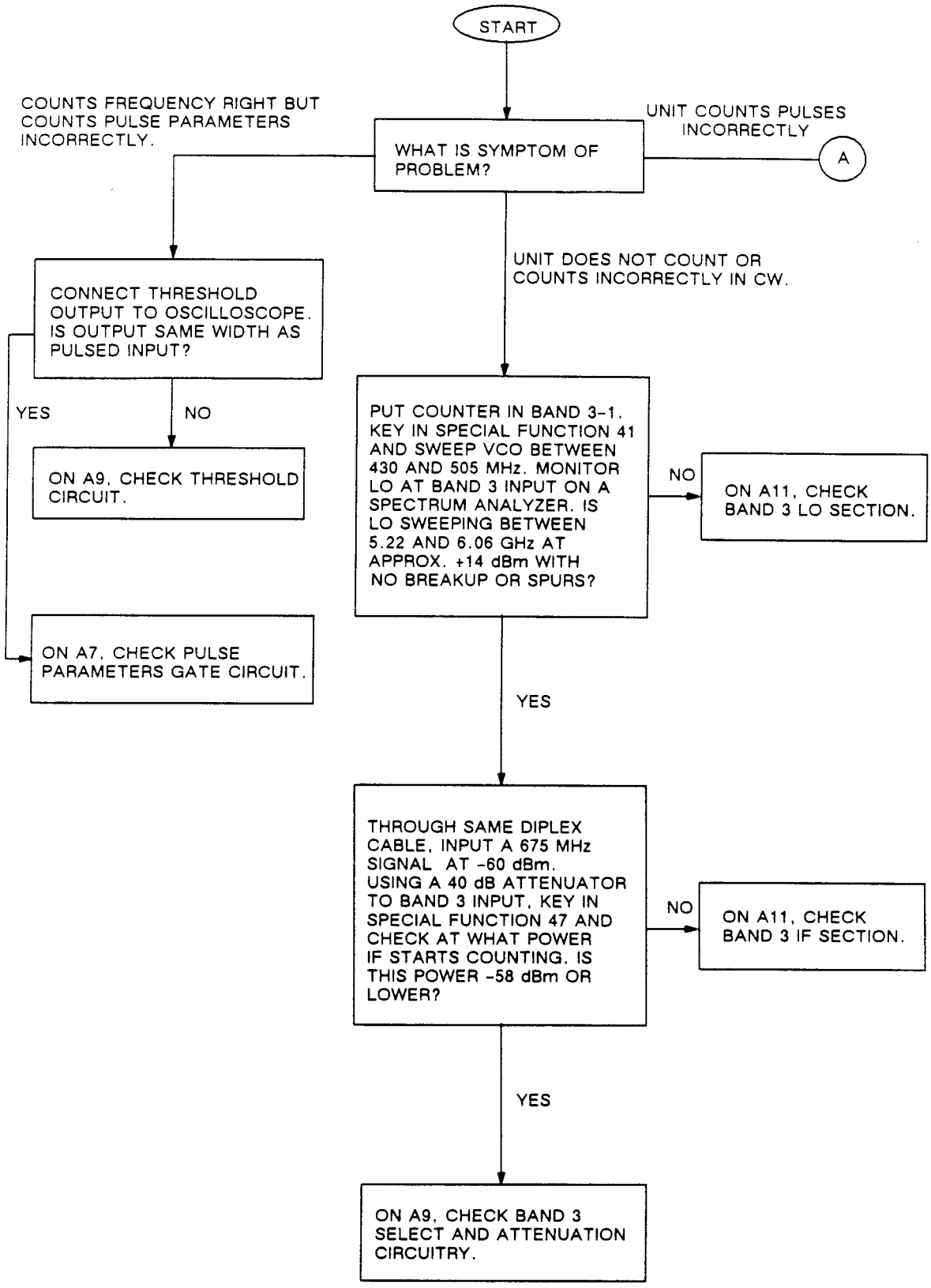

Figure 11-9. Troubleshooting Tree. (Sheet 1 of 2)

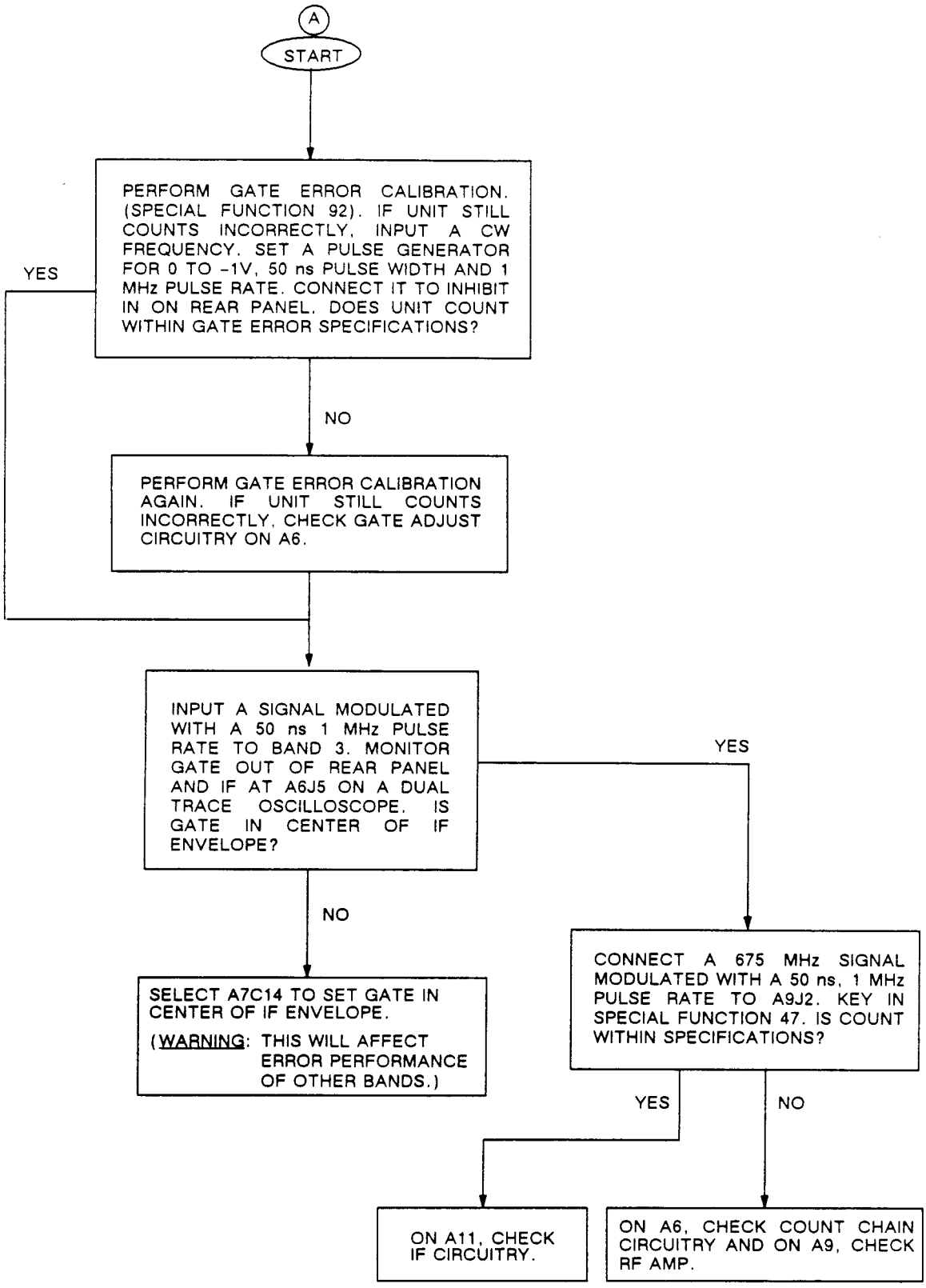

Figure 11-9. Troubleshooting Tree.
(Sheet 2 of 2)

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OPTION 5804, BAND 3 FREQUENCY EXTENSION (CCN 6905) 2010807-01 Rev. B
(CCN 6906, 6907, 6908) 2010807-02 Rev. A

ITEM NO.	DESCRIPTION	EIP NO.	UNITS PER ASSY
1	MODULE ASSY,CONV,MM WAVE,B3,588B **(CCN 6905)**	2010808-01	1
1A	MODULE ASSY,CONV,MM WAVE,B3,588B **(CCN 6906, 6907, 6908)**	2010808-02	1
2	CABLE ASSY,SRC,B3 IN OPT	2040283-01	1
3	CABLE ASSY,COAX,58XB,W6	2040454-01	1
4	CABLE ASSY,COAX,58XB,W12	2L040453-01	1
5	SCR,PNH X-REC SLFLKG 2-32X5/16	5124006-05	3

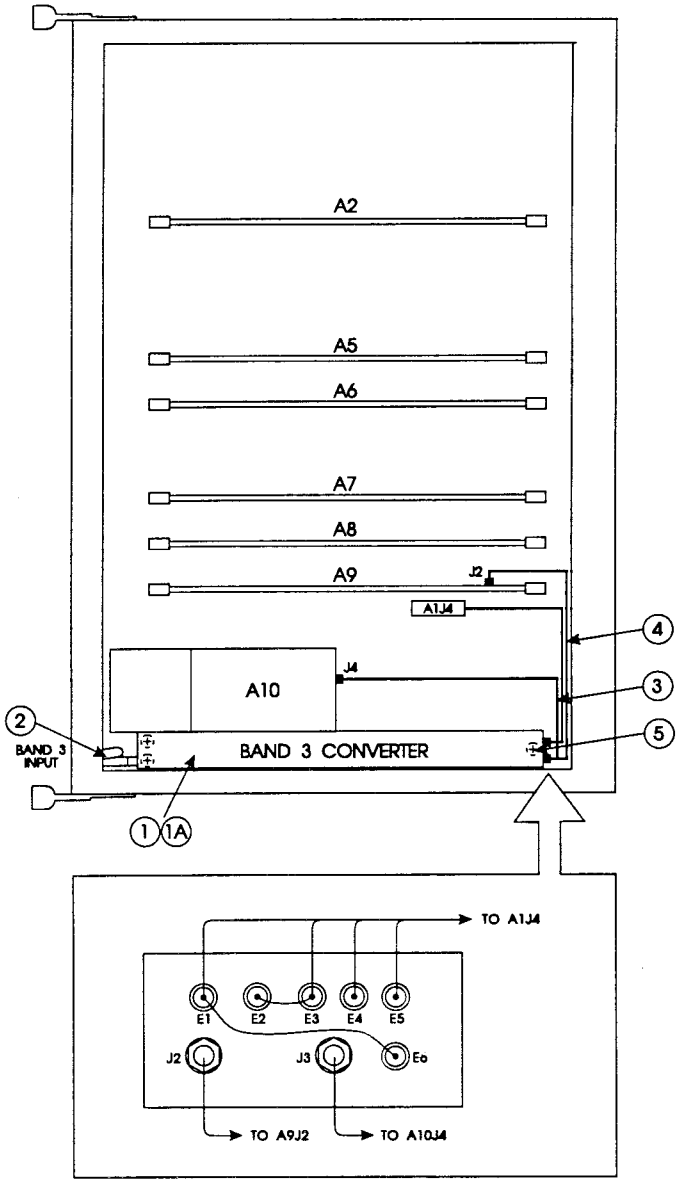

Figure 11-10. Extended Frequency Option Interconnection Diagram.

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OPTIONS 5807, 5808, 5809 AT-CUT OVENIZED HIGH STABILITY TIMEBASES (2010806-01, -02, -03)

NOTE

Options 5807, 5808, and 5809 were discontinued as of December 1992. These discontinued high stability ovenized oscillators incorporated an AT-cut crystal. They were replaced by a new Option 5809 incorporating a SC-cut crystal. The new Option 5809 has virtually identical specifications as the old Option 5809, but requires less warm-up time. Refer to the end of this section for information on the new Option 5809.

Three high stability timebase oscillators (oven oscillators) are available as options on either model 585B or 588B. These options enhance the accuracy of the counter by adding oven-stabilized crystal oscillators. These oscillators improve counter operation by reducing both time and temperature variations.

When any one of these options is installed, the TCXO is removed from gate generator board (A7) and the following components are added.

- One of three oven oscillators mounted on the chassis
- 28 VDC power supply board
- Power supply transformer
- Timebase adjustment control mounted on the rear panel
- Related interconnecting cable harnesses

Table 11-6. Oven Oscillator Option Specifications.

	5807	5808	5809
AGING RATE/24 HOURS (After 72 hour warm-up)	$<5 \times 10^{-9}$	$<1 \times 10^{-9}$	$<5 \times 10^{-10}$
SHORT TERM STABILITY (1 second average)	$<1 \times 10^{-10}$ rms	$<1 \times 10^{-10}$ rms	$<1 \times 10^{-10}$ rms
0 to +50 °C TEMPERATURE STABILITY	$<6 \times 10^{-8}$	$<3 \times 10^{-8}$	$<3 \times 10^{-8}$
±10% LINE VOLTAGE CHANGE	$<5 \times 10^{-10}$	$<2 \times 10^{-10}$	$<2 \times 10^{-10}$

POWER SUPPLY

The oven oscillator power supply is a simple 28 V regulated, current limited power supply. U1 and U2 (Figure 11-14) provide voltage regulation, thermal protection and current limiting.

T1, CR1, C1, and C2 provide a 40 V regulated DC voltage. The output voltage is set by voltage divider R3, R4, and R5. These resistors were selected so that 28 V out provides 2.23 V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground.

The oven oscillator power supply is on and operating as long as the counter is connected to an active ac power source. The counter's POWER STBY/ON switch on the front panel does not control this assembly.

CALIBRATION

When oven oscillator options are installed in the counter, the effects of temperature variations and aging must still be considered, although the magnitudes of the inaccuracies associated with each oscillator are greatly reduced.

Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of ac power). Under these conditions changes in frequency will generally be in the positive direction for either an increase or decrease in temperature from +25 °C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1×10^{-9} parts, relative to a standard, use the procedure illustrated below.

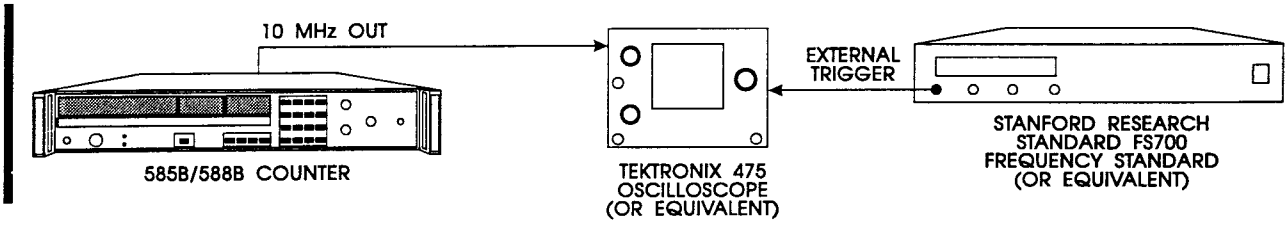

Figure 11-11. Oven Oscillator Calibration Setup.

All frequency checks and adjustments should be made only after the oscillator has been continously powered for 24 hours.

To measure oscillator frequency:

1. Set up the equipment as shown in Figure 11-11 and described below.
2. Connect the counter's internal oscillator output signal from the 10 MHZ IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscillator.
3. Trigger oscilloscope externally with the frequency standard. The VLF comparator is used to determine the absolute frequency of the standard.
4. Set oscilloscope sweep rate to 0.1 µs/cm.
5. Adjust oscilloscope vertical controls for maximum gain.

6. Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T\text{drift of zero crossing}}{T\text{observation time of drift}} = \frac{\Delta f}{f}$$

if the pattern drifts at a rate of 0.01 µs every 10 s the frequency is in error by 1 part in 10^9.

7. Horizontal drift of oscilloscope display in µs/s s a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the 10 MHz ADJ control on the rear panel of the counter until the pattern stops drifting.

NOTE

For higher accuracy, the counter should be operated for 72 hours prior to adjustment.

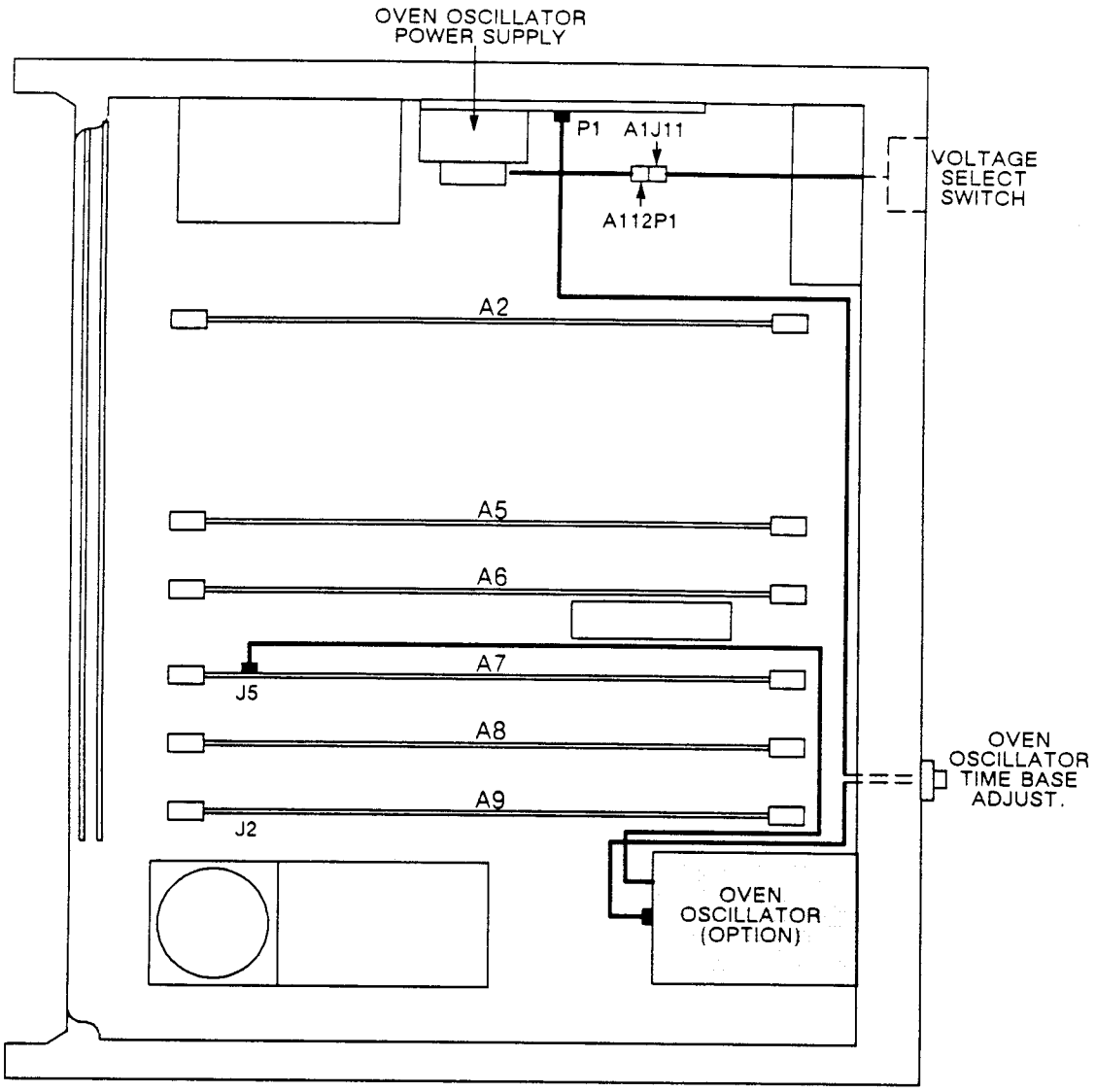

Figure 11-12. Oven Oscillator Interconnection Diagram.

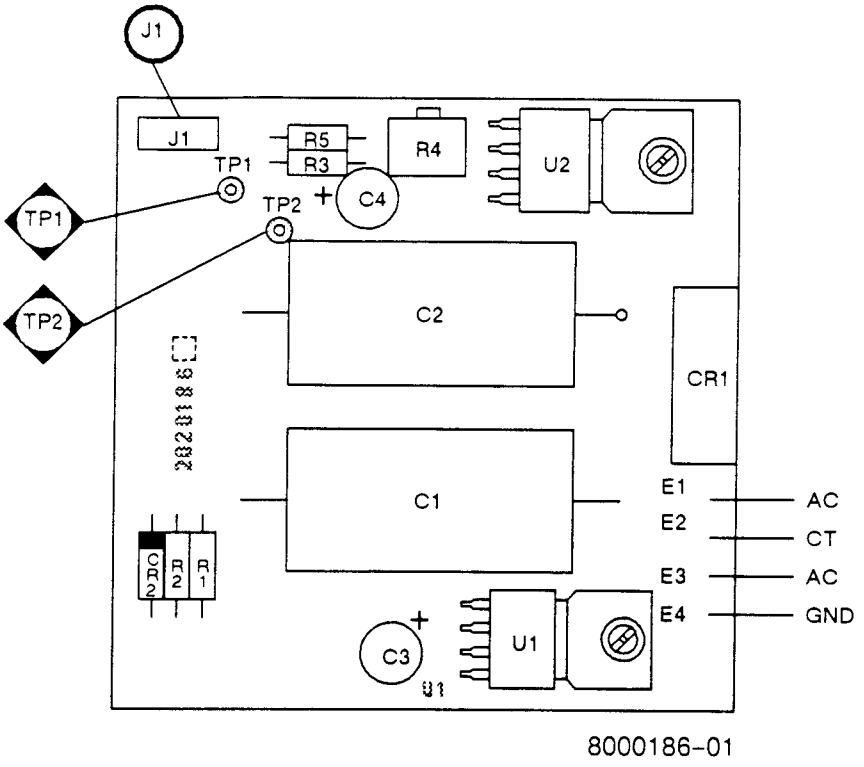

Figure 11-13. Oven Oscillator Power Supply Component Location.

OPTIONS 5807, 5808, 5809 - TIME BASE OSCILLATOR 2020186-01 Rev. D

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ELCTLT	680µF	10%	40V	2200021-00	2
C2	C1						
C3		CAP,TANTALUM	10µF	20%	25V	2300029-00	2
C4	C3						
CR1		DIODE,BR81D,BRIDGE,RECT				2710019-00	1
CR2		DIODE,1N4001,PWR RCT				2704001-00	1
J1		CONN,FRICT LK .100,3 PIN				2620121-00	1
R1		RES,M/OX	3.3K	1/4W	2%	4130332-00	1
R2		RES,M/OX	2K	1/4W	2%	4130202-00	1
R3		RES,M/OX	560	1/4W	2%	4130561-00	1
R4		POT,CERMET	500	0.5W	10%	4250014-00	1
R5		RES,M/OX	3.6K	1/4W	2%	4130362-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	2
TP2	TP1						
U1		IC,UA78MG,VOLT RGLTR,POS,40V				3040780-00	1
U2		IC,UA79MG,VOLT RGLTR,NEG,40V				3040790-00	1
HARDWARE USED IN THIS ASSEMBLY							
		NUT,HEX,SM-PATT,CRES 4-40 UNC-2B				5182004-40	2
		WASH,LK,SPLIT,CRES #4				5162004-00	2
		WASHER,FLAT,CRES,REDUCED O.D. #4				5161004-00	2
		SCR,PNH X-REC 4-40X1/4 UNC				5120004-04	2

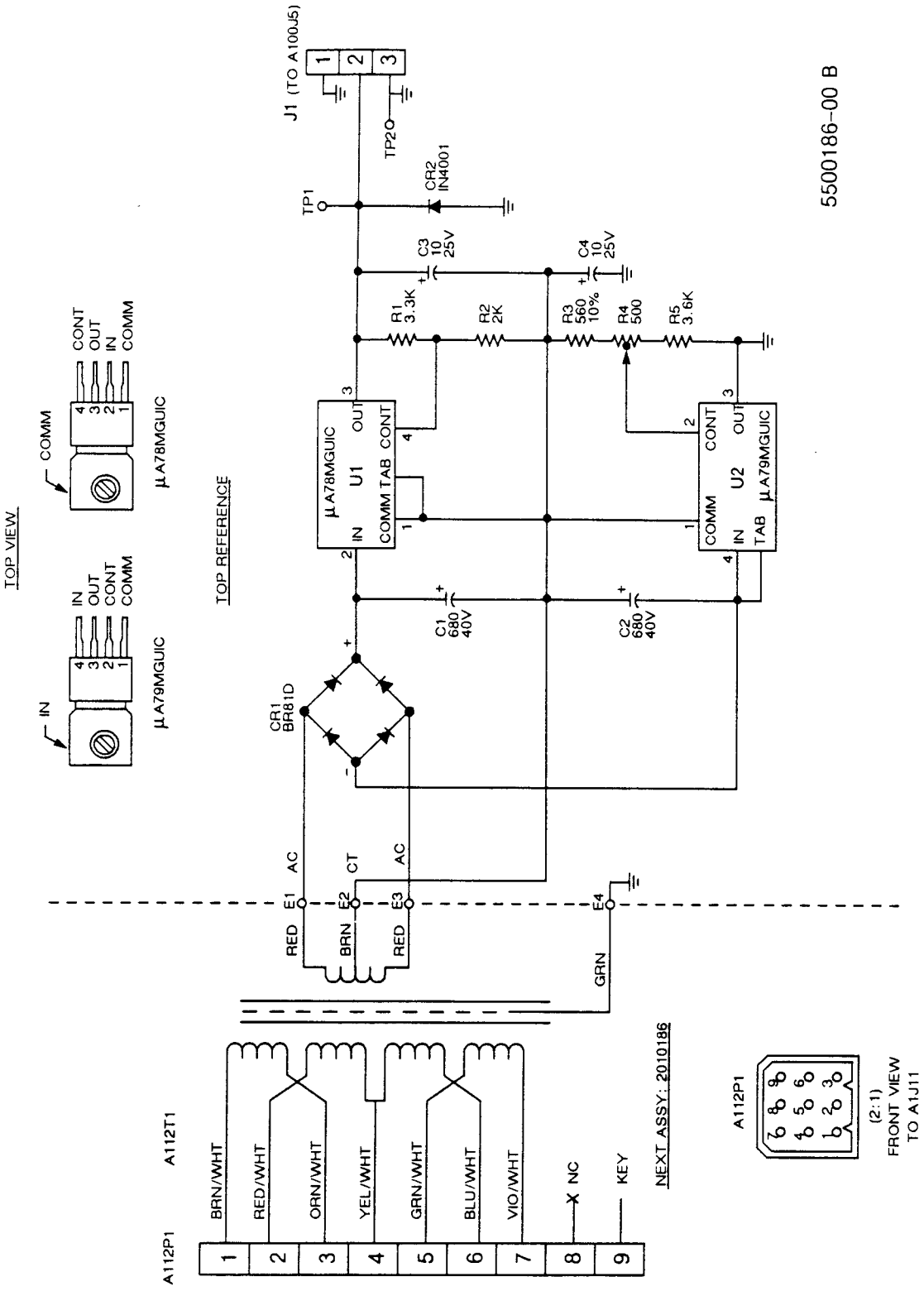

Figure 11-14. Oven Oscillator Option Schematic Diagram.

OPTION 5809
SC-CUT OVENIZED HIGH STABILITY TIMEBASE
2010806-04

NOTE

Options 5807, 5808, and 5809 were discontinued as of December 1992. These discontinued high stability ovenized oscillators incorporated an AT-cut crystal. They were replaced by this new Option 5809 incorporating a SC-cut crystal. The new Option 5809 has virtually identical specifications as the old Option 5809, but requires less warm-up time.

INTRODUCTION

The optional high stability oven oscillator improves counter measurement accuracy by minimizing frequency error caused by long-term frequency drift (aging rate), while providing both improved short-term stability and temperature stability. These improvements occur because the oven oscillator crystal is housed in a proportional control oven which maintains the crystal at an elevated temperature, reducing the effects of changes in ambient temperature on oscillator frequency output. The oven is energized whenever the counter line cord is connected to an ac power source.

SPECIFICATIONS

Frequency	10 MHz
Aging rate	$<5 \times 10^{-10}$/day, 1×10^{-7}/year
Short term stability	$<1 \times 10^{-10}$ rms for one second averaging time
Temperature stability	$<3 \times 10^{-8}$ over the range of 0 to 50 °C
Line variation	$<1x\ 10^{-9}$ for ±10% line voltage change
Phase noise	-120 dBc/Hz at 10 Hz from carrier
Warm-up time	One hour
Retrace	$<5 \times 10^{-9}$ of final value 10 minutes after turn-on at 25 °C $<1 \times 10^{-9}$ of final value 30 minutes after turn-on at 25 °C

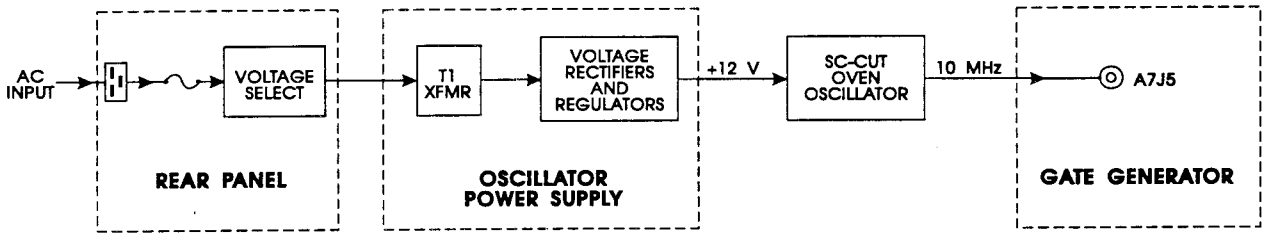

Figure 11-15. Oven Oscillator Block Diagram.

TIMEBASE CALIBRATION

The accuracy of the oven oscillator directly affects the measurement accuracy of the 585B/588B counter. From the time an oscillator is set to its specified frequency, it will begin drifting. The magnitude of the frequency drift is specified as the aging rate of the oscillator. Timebase calibration removes the frequency error due to the aging rate of the oscillator. To maintain an accuracy of ±2 kHz on a 20 GHz measurement, calibration of the timebase is recommended once every 12 months.

NOTE

Calibration of the timebase should be made only after the oscillator has been continuously operated for a minimum of one hour, allowing for stabilization of the oscillator.

EQUIPMENT REQUIREMENTS

Equipment used for calibrating the oven oscillator is listed in Table 11-7. The critical parameters are the minimum use specifications required for the performance of the calibration, and are included to assist in the selection of alternative equipment. Satisfactory performance of alternative items should be verified prior to use. All applicable equipment must bear evidence of current calibration.

Table 11-7. Recommended Equipment.

Description	Critical Parameters	Manufacturer	Model
Frequency standard	10^{-10} short-term stability	Stanford Research Systems	FS700
Oscilloscope	100 MHz	Tektronix	475
50 ohm termination		Pomona	4119-50

Description

In the following procedure, the timebase is calibrated against a frequency standard, using an oscilloscope. The 10 MHz frequency standard is used to trigger the oscilloscope while the 10 MHz signal from the counter is applied to channel 1 of the oscilloscope. Since the oscilloscope is triggered by the frequency standard, any difference in frequency between the 10 MHz frequency standard and the 10 MHz from the counter causes the displayed signal trace to move to the left or to the right. The rate of the signal trace movement is directly proportional to the frequency difference between the frequency standard and the timebase in the counter. The fractional timebase error can be calculated using the following formula:

Fractional Timebase Error = (movement in cm per second) x (time per division)

For example, if the sweep speed of the oscilloscope is set to 1 µs per division, and the signal is drifting at a rate of 2 cm per second, then the fractional timebase error is calculated as follows:

$$\text{Fractional Timebase Error} = \frac{2\ \text{cm}}{\text{s}} \times \frac{1 \times 10^{-6}}{\text{cm}} = 2 \times 10^{-6}$$

The actual timebase error in Hz is calculated by multiplying the fractional timebase error by the frequency of the frequency standard, as follows:

$$\text{Timebase Error (Hz)} = \pm[(2 \times 10^{-6}) \times (10 \times 10^{6})] = \pm 20\ \text{Hz}$$

The counter measurement error is calculated by multiplying the fractional timebase error by the frequency of the signal being measured. For example, if the fractional timebase error is 2×10^{-6}, then the measurement error on a 20 GHz signal is calculated as follows:

$$\text{Measurement Error (Hz)} = \pm[(2 \times 10^{-6}) \times (20 \times 10^{9})] = \pm 40 \text{ kHz}$$

Equipment

Frequency standard (Stanford Research Systems FS700)
Oscilloscope (Tektronix 475)
50 ohm termination (Pomona 4119-50)

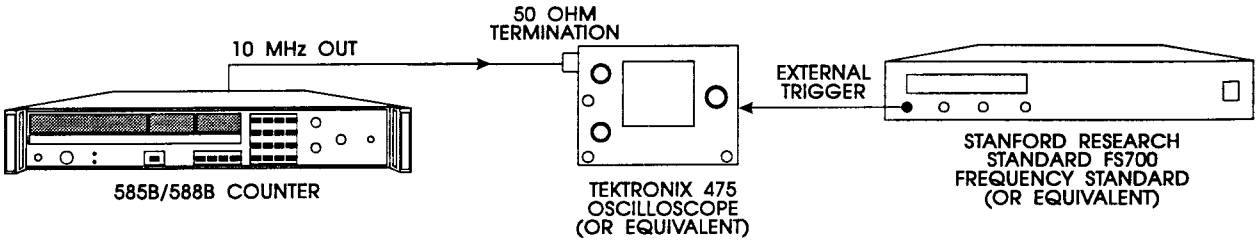

Figure 11-16. Timebase Calibration Setup.

Procedure

1. Turn on the EIP 585B/588B counter and allow a warm-up period of at least six hours prior to calibrating the timebase.
2. Set up the equipment as shown in Figure 11-16 and as described below.
3. Connect the frequency standard output to the external trigger input on the oscilloscope. Connect the 10 MHz IN/OUT connector from the rear panel of the 585B/588B to the channel 1 input of the oscilloscope.
4. Set the oscilloscope to external trigger.
5. Set the oscilloscope sweep speed to 0.01 µs per cm.
6. While monitoring the 10 MHz timebase signal from the 585B/588B on the oscilloscope, adjust the frequency of the timebase by turning the adjustment located under the oven oscillator cap screw (refer to Figure 11-17) until the horizontal movement rate is ≤1 centimeter in 10 seconds. This sets the timebase to an accuracy of 1×10^{-9} (10 MHz ±50 mHz).

POWER SUPPLY THEORY OF OPERATION

The oven oscillator power supply is a 12 V regulated, current limiting supply. U1 provides voltage regulation, thermal protection and current limiting. T1, CR1, and C1 provide a 40 V nominal unregulated DC voltage. Diode CR2 protects the supply from being pulled more negative than ground.

The oven oscillator power supply is on and operating as long as the counter is connected to an active ac power source. The counter's POWER STBY/ON switch on the front panel does not control this assembly.

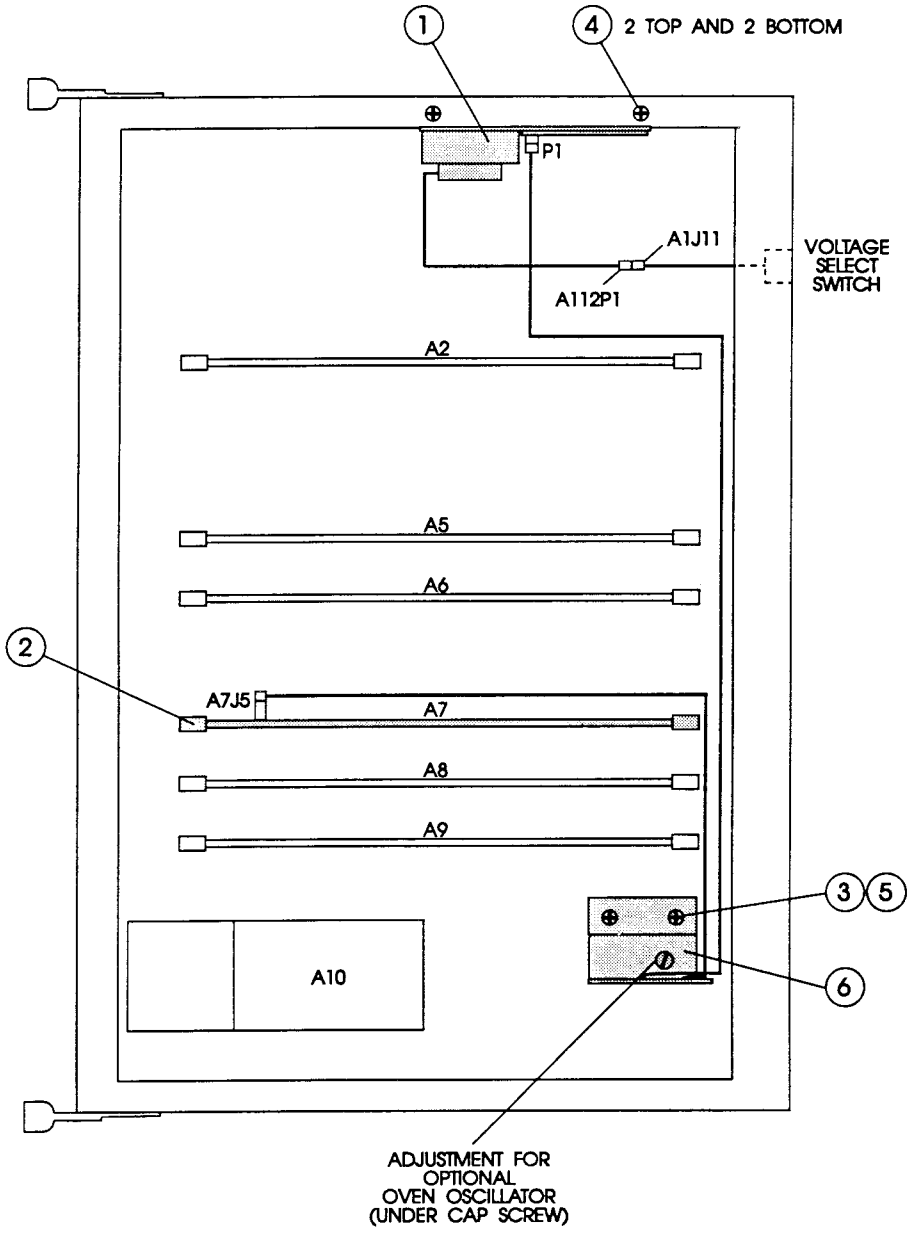

Figure 11-17. Oven Oscillator Connection Diagram.

OPTION 5809 SC-CUT OVENIZED HIGH STABILITY TIMEBASE 2010806-04

ITEM NO.	DESCRIPTION	EIP NO.	UNITS PER ASSY
1	OVEN OSC,PWR SUPPLY	2010226-03	1
2	PCB ASSY,GATE GENERATOR	2020407-01	1
3	WASHER,FLAT,CRES NO. 6	5160006-00	2
4	SCR,PNH X-REC 6-32X1/4 UNC	5120006-04	4
5	SCR,PNH X-REC SLFLKG 6-32X3/8 UNC	5126006-06	2
6	PCB ASSY,OVEN OSC	2020479-04	1

NOTE

PCB assembly 2020407-01, item number 2 on the above parts list, replaces PCB assembly 2020217-04 (A7) when the optional oven oscillator is installed. PCB 2020407-01 is identical to 2020217-04 with the following exceptions:

- C14 is CAP,DISC,CER 180PF 10% 100V 2150046-00 1
  SEE NOTE 1
- R60 is RES,SMD 39.2 1/8W 1% 4233929-00 1
- C32 is not installed on 2020407-01.
- TP6 is installed and is the same as TP1.
- TCXO Y1 is not installed on 2020407-01.
- Connector J5 is installed on 2020407-01.

A portion of the schematic of the Gate Generator (A7) circuitry is illustrated below, showing the modifications performed when the oven oscillator option is installed.

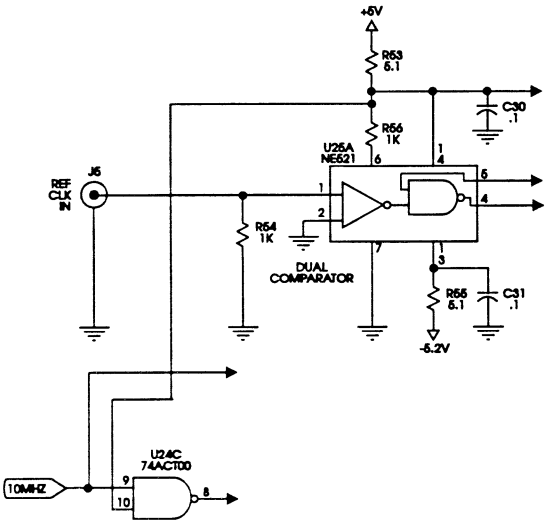

Figure 11-18. Gate Generator Modifications for Option 5809.

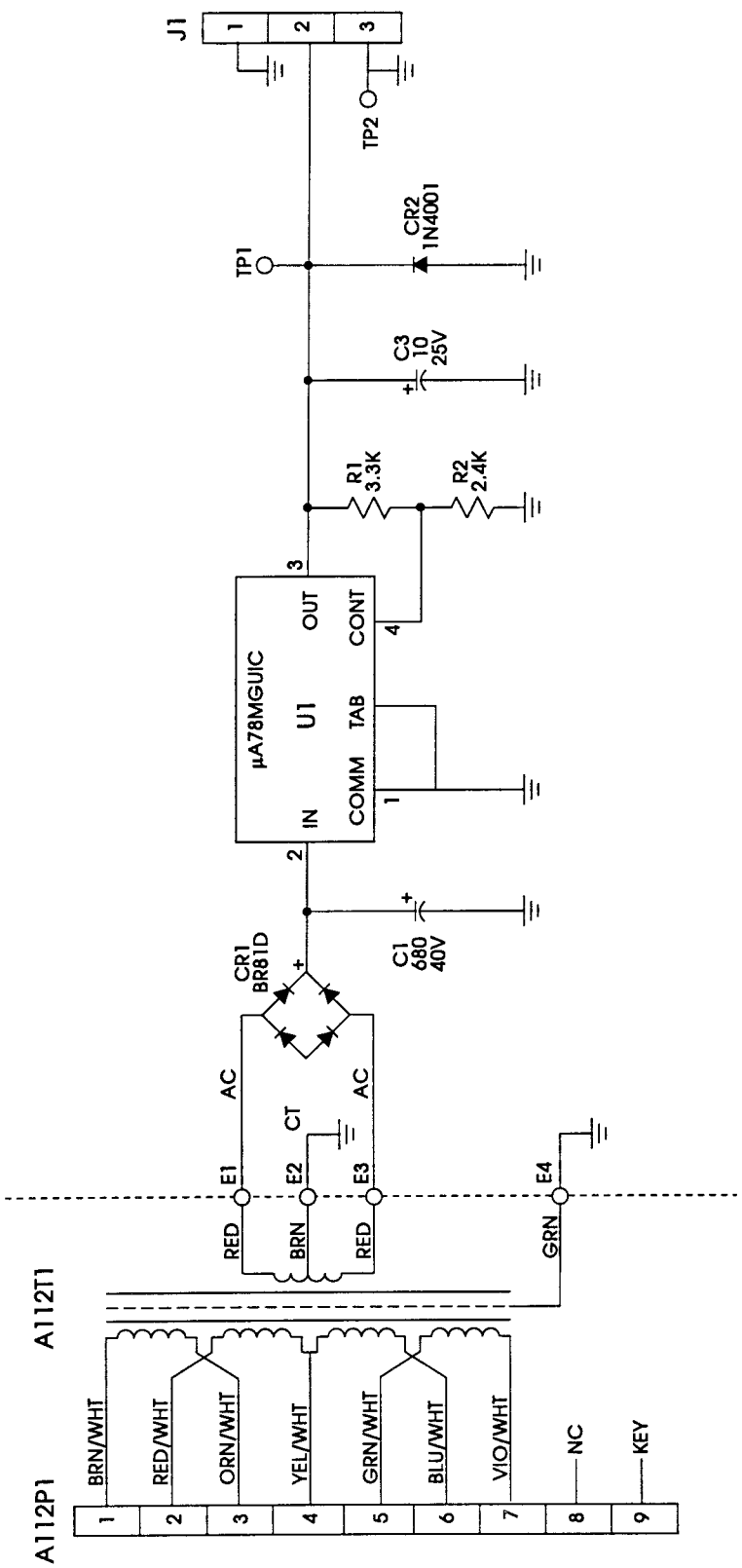

Figure 11-19. Oven Oscillataor Option Schematic Diagram.

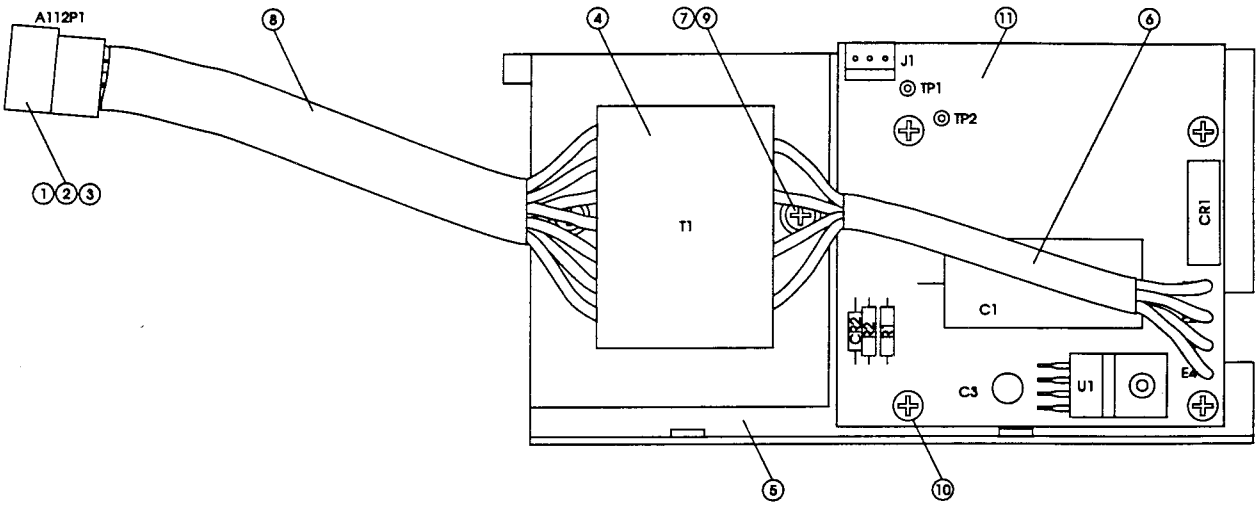

Figure 11-20. Option 5809 Power Supply Assembly.

OPTION 5809 POWER SUPPLY ASSEMBLY 2010226-03 Rev. B

ITEM NO./ REF. DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
1		CONN,PLUG,MINTR,9 PIN,W/O				2620112-00	1
2		CONN,CONTACT,MALE				2620038-00	1
3		CONN,CONTACT,FEM				2L620036-00	8
4		XFMR,PWR,OSC				4900006-00	1
5		BRACKET,OVEN OSC				5210376-02	1
6		TUBING,SHRINK,1/4 BLK				5480003-00	2.5 IN.
7		WASHER,FLAT,FIBRE #4				5000136-00	2
8		TUBING,SHRINK,3/8 BLK				5480004-00	3.5 IN.
9		SCR,PNH X-REC 4-40X1 UNC				5120004-16	2
10		SCR,PNH,X-REC,SEMS,INTL,4-40X1/4				5171004-04	4
11		PCB ASSY,OSC PWR SPLY				2020186-02	1
COMPONENTS IN PCB ASSY							
C1		CAP,ELCTLT	680µF	10%	40v	2200021-00	1
C2		NOT USED					
C3		CAP,TANTALUM	10µF	20%	25v	2300029-00	1
CR1		DIODE,BR81D,BRIDGE,RECT				2710019-00	1
CR2		DIODE,1N4001,PWR RCT				2704001-00	1
J1		CONN,FRICT LK .100,3 PIN				2620121-00	1
R1		RES,M/OX	3.3K	1/4W	2%	4130332-00	1
R2		RES,M/OX	2.4K	1/4W	2%	4130242-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	2
TP2	TP1						
U1		IC,UA78MG,VOLT RGLTR,POS,40V				3040780-00	1
HARDWARE USED IN THE PCB ASSEMBLY							
		NUT,HEX,SM-PATT,CRES 4-40 UNC-2B				5182004-40	2
		WASHER,LK,SPLIT,CRES #4				5162004-00	2
		WASHER,FLAT,CRES,REDUCED O.D. #4				5161004-00	2
		SCR,PNH X-REC 4-40X1/4 UNC				5120004-04	2

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QUICK REFERENCE LIST OF GPIB COMMAND MESSAGES

CONTROL MESSAGES

Header	Argument	Terminator	Description
CLEARDISPLAY	None	None	Returns the display to normal measurement results display, clear error. (Equivalent to front panel CLEAR DISPLAY key.)
INITIALIZE	"	"	Reconfigures the instrument to power-on state. (Equivalent to front panel INIT/LOCALkey.)
RESET	"	"	Resets counter to restart a new signal measurement cycle. (Equivalent to front panel RESET key.)
TRIGGER	"	"	Triggers a new measurement cycle. (Equivalent to front panel TRIG key.)

MODE MESSAGES

Header	Argument	Terminator	Description
DYNAMIC	ON or OFF	None	Suppresses blanks when counter is configured in talker mode for faster free-field data transfer.
EXTERNAL	"	"	Controls the INT/EXT time base reference. (Special Function 08 can also be used to select the external time-base.)
HEADER	"	"	Adds an alpha header and terminator for talker.
HOLD	"	"	Holds the last result if on. (Equivalent to front panel HOLD.)
PERIOD	"	"	Turns pulse period measurement on or off or DEFAULT. (Equivalent to front panel PULSE PERIOD key.)
SCIENTIFIC	"	"	Selects scientific notation for talker.
SEPARATE	"	"	Replaces the commas with CR LF between multinumber results.
WIDTH	"	"	Turns pulse width measurement on or off. (Equivalent to front panel PULSE WIDTH key.)

PARAMETER MESSAGES

Header	Argument	Terminator	Description
AVERAGE	<number>	None	Inputs an averaging value (01 to 99).
BAND	"	"	Selects a specific band (0 to 3) or DEFAULT.
CENTERFREQ	"	(Hz/kHz/MHz/GHz)	Sets a center frequency value and mode.
FETCH	"	None	Recalls counter setup stored in specified storage register (0 to 9). (Special Function 73.)
HIGHLIMIT	"	(Hz/kHz/MHz/GHz)	Sets a frequency limit high value.
LOWLIMIT	"	"	Sets a frequency limit low value.
MEMORY	<hex_adrs>	<hex_data>	Accesses a memory location and alters it (altering is optional). (Special Function 46.)
MEMORY	INCREMENT	"	Accesses the next memory location. (Special Function 46.)
MEMORY	DECREMENT	"	Accesses the previous memory location. (Special Function 46.)
MINPRF	<number>	(Hz/kHz/MHz/GHz)	Sets a minimum PRF value.
MULTIPLIER	"	None	Inputs a multiplier value (01 to 99).
OFFSETFREQ	"	(Hz/kHz/MHz/GHz)	Sets a frequency offset value.
RESOLUTION	"	None	Sets the frequency measurement resolution (0 to 9).
SAMPLERATE	"	(s/ms)	Sets a delay between measurement values (0 to 100 sec, 10 ms resolution).
SPECIAL	"	None	Activates a specific special function (00 to 99).

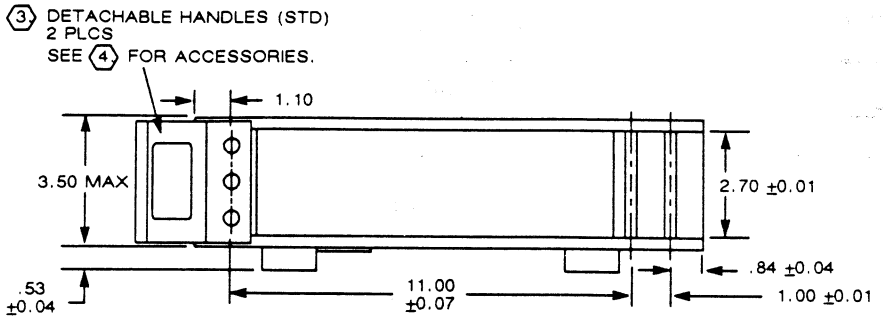
QUICK REFERENCE LIST OF GPIB COMMAND MESSAGES (Continued)

PARAMETER MESSAGES (Continued)

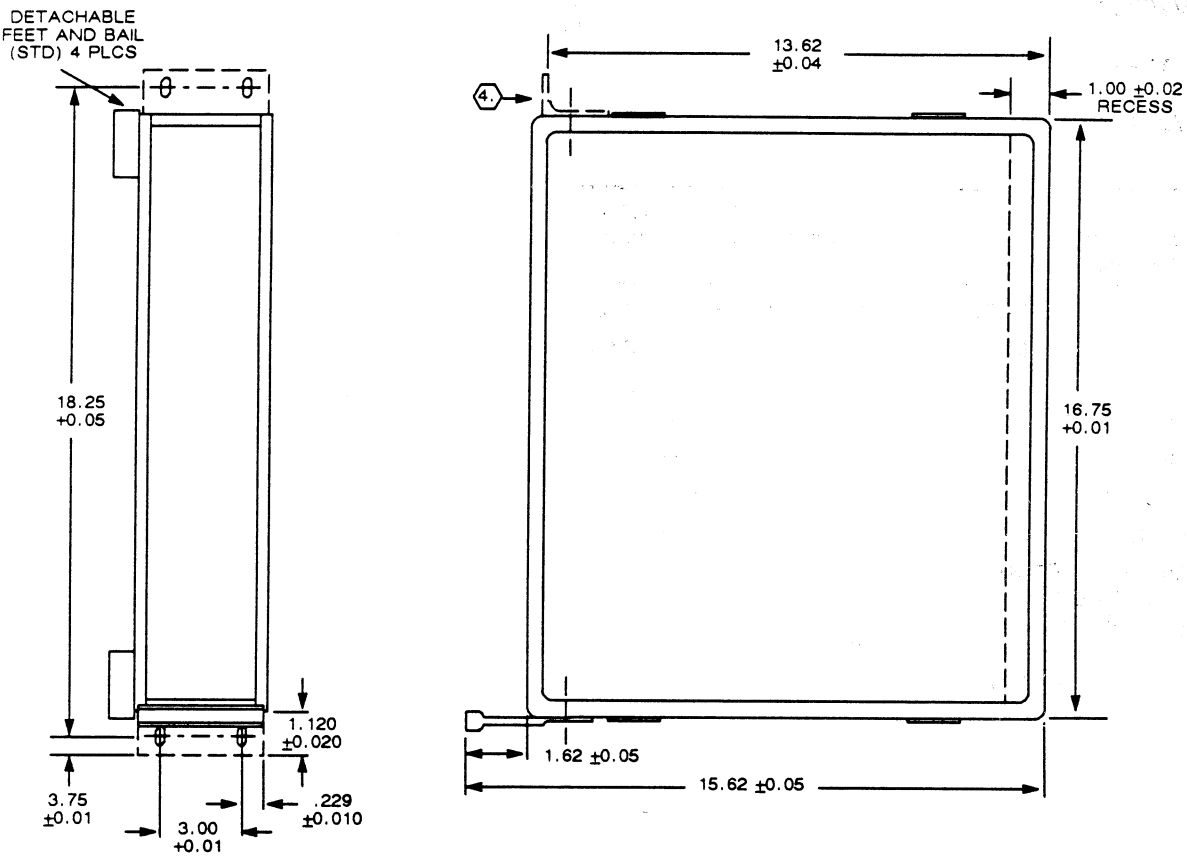
Header	Argument	Terminator	Description
SRQMASK	<number>	None	Selects the ORed combination of status events to cause a service request.
STORE	"	"	Stores current counter setup in specified storage register (0 to 9). (See Special Function 72.)
SUBBAND	"	"	Selects a specific Band 3 subband (1 to 6)
V1FREQ	"	(Hz/kHz/MHz/GHz)	Sets a start frequency for VCO sweep (Special Functions 41, 42).
V2FREQ	"	"	Sets a stop frequency for VCO sweep (Special Functions 41, 42).
Y1FREQ	"	"	Sets a start frequency for YIG sweep (Special Function 40).
Y2FREQ	"	"	Sets a stop frequency for YIG sweep (Special Function 40).

OUTPUT CONTROL MESSAGES

Command	Description
OUTPUT AVERAGE	Outputs the last specified averaging value.
OUTPUT BAND	Outputs the number of the last specified band.
OUTPUT CENTERFREQ	Outputs the center frequency last specified.
OUTPUT CONFIGURATION	Outputs current configuration of instrument. See page 4-13.
OUTPUT DATE	Outputs a 42-character string that shows the revision level and date.
OUTPUT DEFAULT	Outputs displayed data.
OUTPUT ERRORNUMBER	Outputs the number of the last error. See listing of error numbers on page 3-35.
OUTPUT FREQUENCY (AND WIDTH) (AND PERIOD)	Controls which measurement results to output. (Note: More than one measurement result is optional. The order of the results is preserved in the output. Output frequency, width and period can be used in any combination.)
OUTPUT HIGHLIMIT	Outputs the high frequency limit last specified.
OUTPUT IDENTIFICATION	Outputs "EIP58nB GPIB dd", where n is 5 or 8 and dd is the GPIB address.
OUTPUT KEYCODE	Outputs the code of the last key pressed.
OUTPUT LEVEL	Outputs the rough amplitude measurement result (Special Function 20).
OUTPUT LOWLIMIT	Outputs the low frequency limit last specified.
OUTPUT MEMORY	Outputs the content of the memory in the last accessed location. (Special Function 41.)
OUTPUT MINPRF	Outputs the minimum PRF last specified.
OUTPUT MULTIPLIER	Outputs the last specified multiplier value.
OUTPUT OFFSETFREQ	Outputs the offset frequency last specified.
OUTPUT RESOLUTION	Outputs the last specified frequency measurement resolution.
OUTPUT SAMPLERATE	Outputs the last specified delay time between measurement values.
OUTPUT SETUP	Outputs a 142-character string that describes the current setup. See page 4-6.
OUTPUT SRQMASK	Outputs the combination of status events required to cause a service request. See page 4-11.
OUTPUT SUBBAND	Outputs the number of the last specified subband.
OUTPUT V1FREQ	Outputs the last specified start frequency for VCO sweep (Special Function 41).
OUTPUT V2FREQ	Outputs the last specified stop frequency for VCO sweep.
OUTPUT Y1FREQ	Outputs the last specified start frequency for YIG sweep (Special Function 40).
OUTPUT Y2FREQ	Outputs the last specified stop frequency for YIG sweep (Special Function 41).



SIDE VIEW



FRONT VIEW

TOP VIEW

PHYSICAL DESCRIPTION

1. Weight: Net 35 lbs.
2. Enclosure: Die cast alum alloy top and bottom frame painted black, extruded alum corner posts with vinyl covered steel side panels. Top and bottom covers are vinyl covered steel. Rear panel is alum with nomenclature screened in black. Front panel is alum with mylar overlay and chrome painted trim strips.

(3.) Removable handles supplied with instrument.

(4.) Accessory kits available: Rack mount angles.
Rack mount angles with handles
Slide mount.